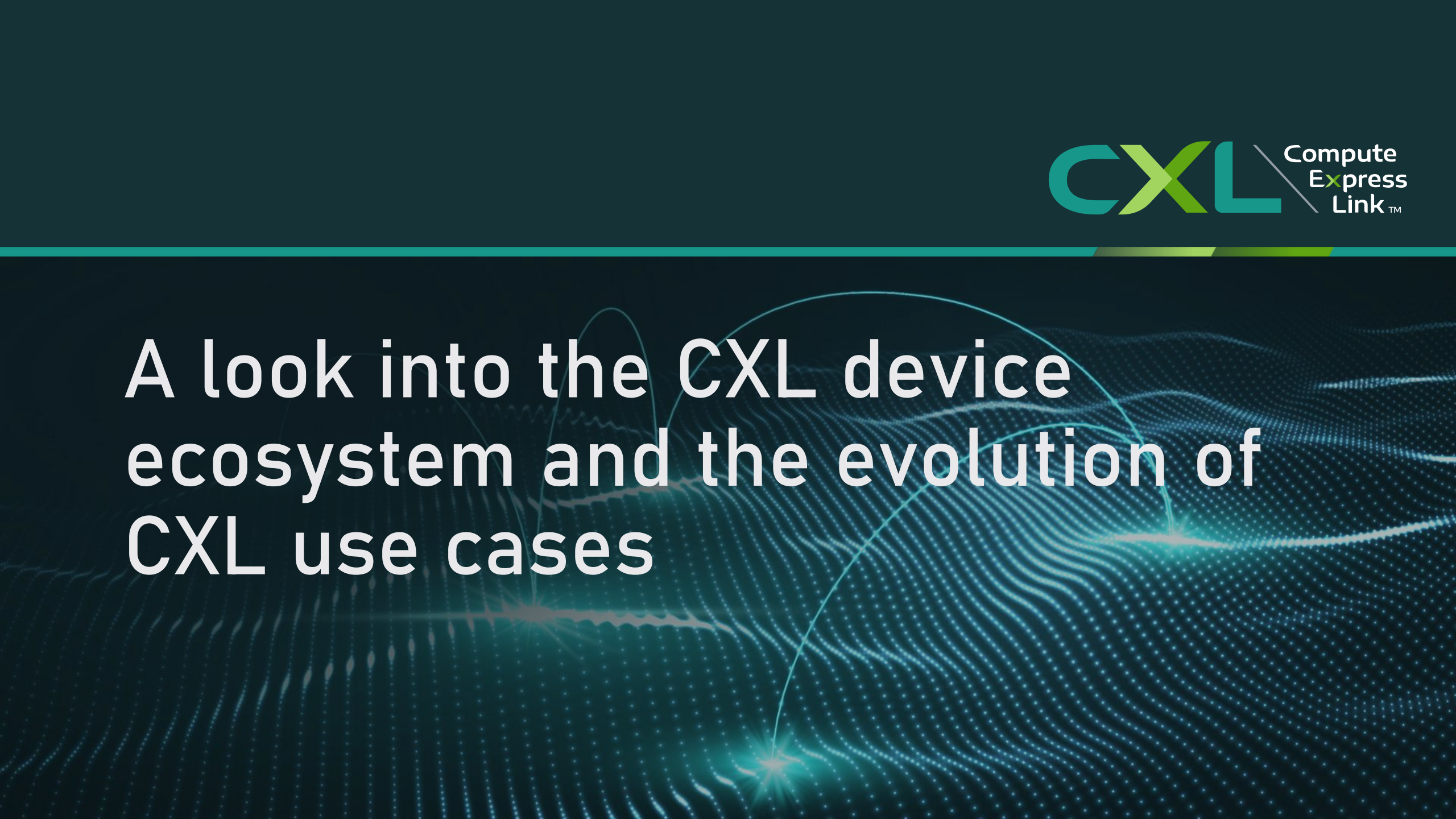
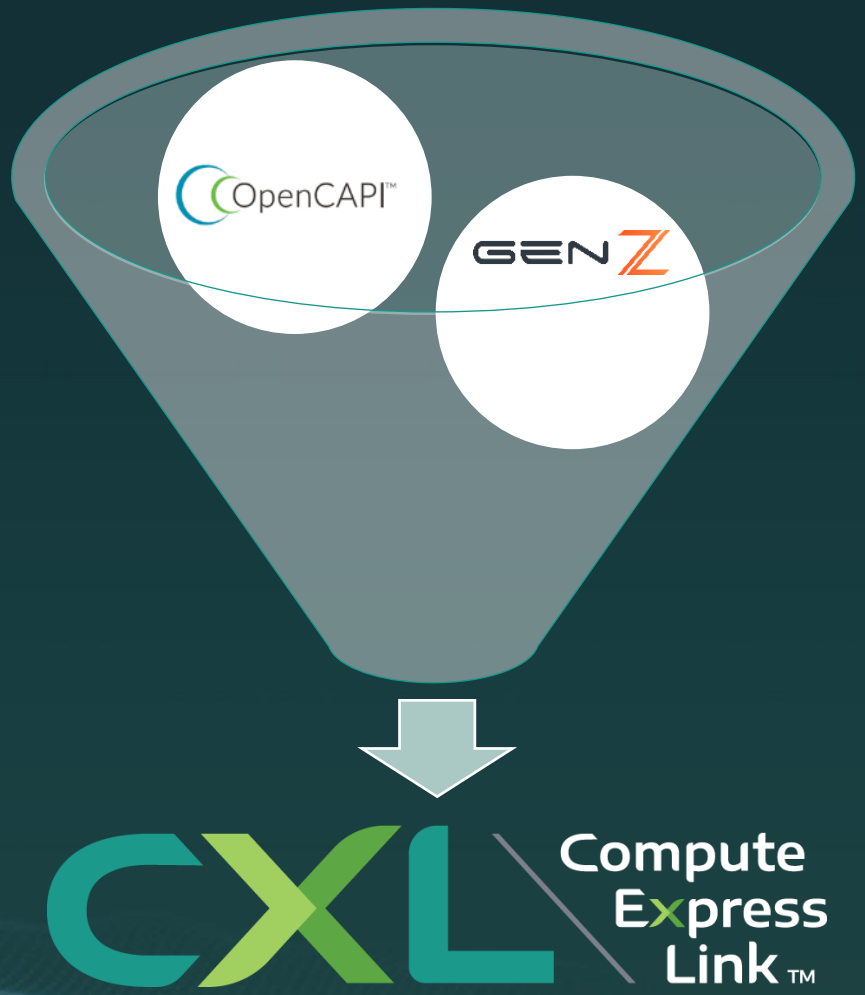

CXL
Compute
Express
Link™
A look into the CXL device ecosystem and the evolution of CXL use cases

CXL Board of Directors

Industry Open Standard for High Speed Communications

240+ Member Companies

Industry focal point



CXL is emerging as the industry focal point for coherent IO

- CXL Consortium and OpenCAPI sign letter of intent to transfer OpenCAPI specification and assets to the CXL Consortium

CXL Compute Express Link™ OpenCAPI™

August 1, 2022, Flash Memory Summit
CXL Consortium and OpenCAPI Consortium Sign Letter of Intent to Transfer OpenCAPI Assets to CXL

- In February 2022, CXL Consortium and Gen-Z Consortium signed agreement to transfer Gen-Z specification and assets to CXL Consortium

Industry Liaisons

CXL is collaborating with industry organizations

CXL Delivers the Right Features & Architecture

Challenges

Industry trends driving demand for faster data processing and next-gen data center performance

Increasing demand for heterogeneous computing and server disaggregation

Need for increased memory capacity and bandwidth

Lack of open industry standard to address next-gen interconnect challenges

CXL

An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

Coherent Interface

Leverages PCIe™ with 3 mix-and-match protocols

Low Latency

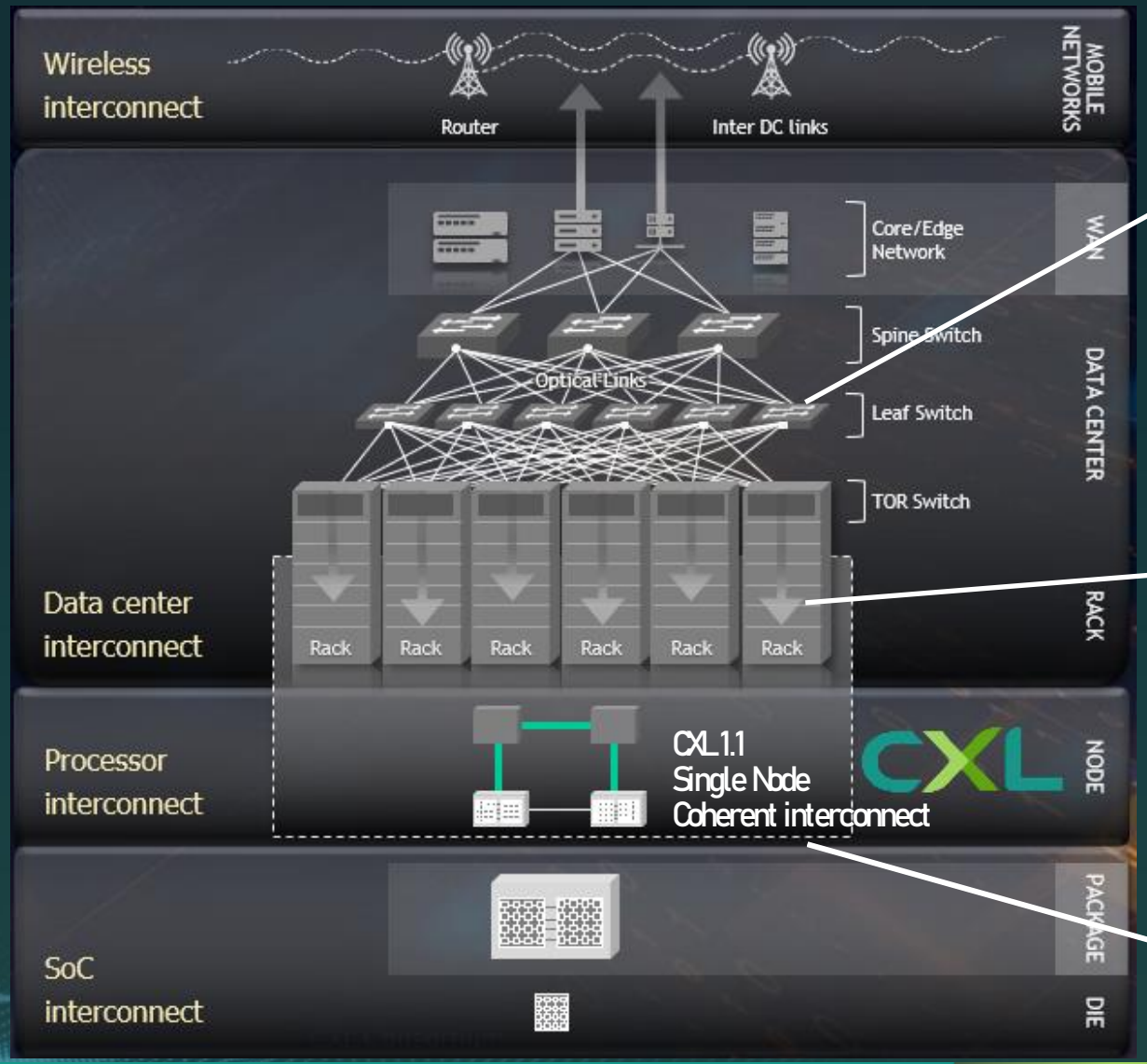
.Cache and .Memory targeted at near CPU cache coherent latency

Asymmetric Complexity

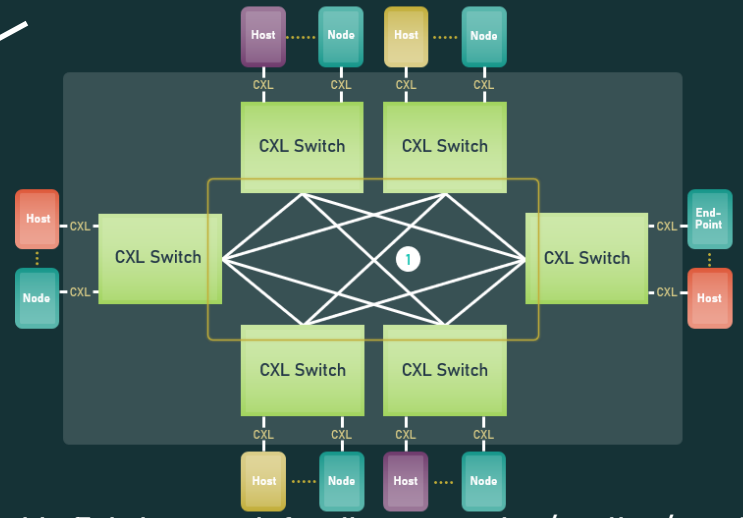
Eases burdens of cache coherent interface designs

www.ComputeExpressLink.org

Data Center: Expanding Scope of CXL



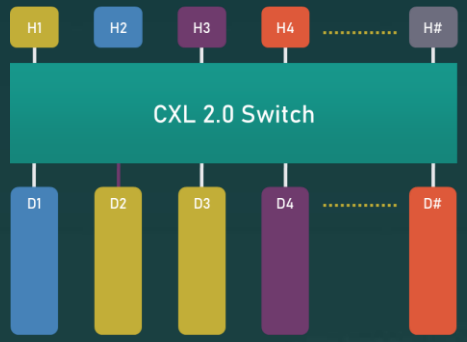
CXL 3.0



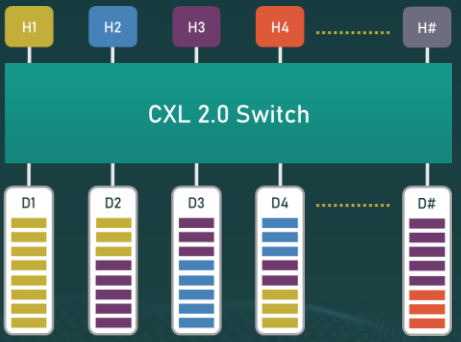
Composable Fabric growth for disaggregation/pooling/accelerator

CXL 2.0

Memory/Accelerator Pooling with Single Logical Devices



Memory Pooling with Multiple Logical Devices



Multiple Nodes inside a Rack/ Chassis supporting pooling of resources

CXL Spec Feature Summary

Features	CXL 1.0 / 1.1	CXL 2.0	CXL 3.0
Release date	2019	2020	August 2022
Max link rate	32GTs	32GTs	64GTs
Flit 68 byte (up to 32 GTs)	✓	✓	✓
Flit 256 byte (up to 64 GTs)			✓
Type 1, Type 2 and Type 3 Devices	✓	✓	✓
Memory Pooling w/ MLDs		✓	✓
Global Persistent Flush		✓	✓
CXL Integrity and Data Encryption (IDE)		✓	✓
Switching (Single-level)		✓	✓
Switching (Multi-level)			✓
Direct memory access for peer-to-peer			✓
Enhanced coherency (256 byte flit)			✓
Memory sharing (256 byte flit)			✓
Multiple Type 1/Type 2 devices per root port			✓
Fabric capabilities (256 byte flit)			✓

	Not supported
✓	Supported

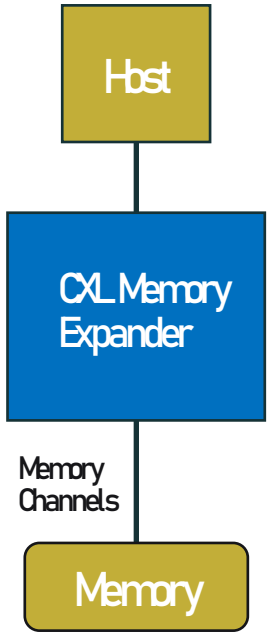
CXL Ecosystem & Demos and Evolving Use Cases

CXL Ecosystem

Growth of CXL Ecosystem since its inception

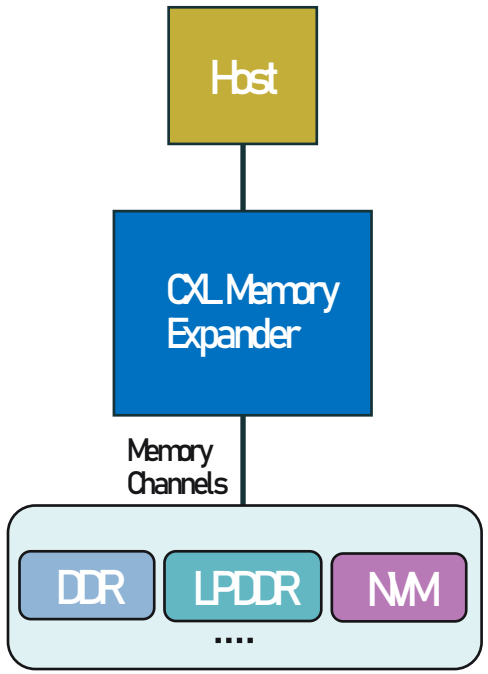
- Ecosystem that meets the ever-increasing performance and scale requirements
- Fully backwards compatible
- Lowers overall system cost
- Comprehensive compliance and testing support

Evolving Use Cases



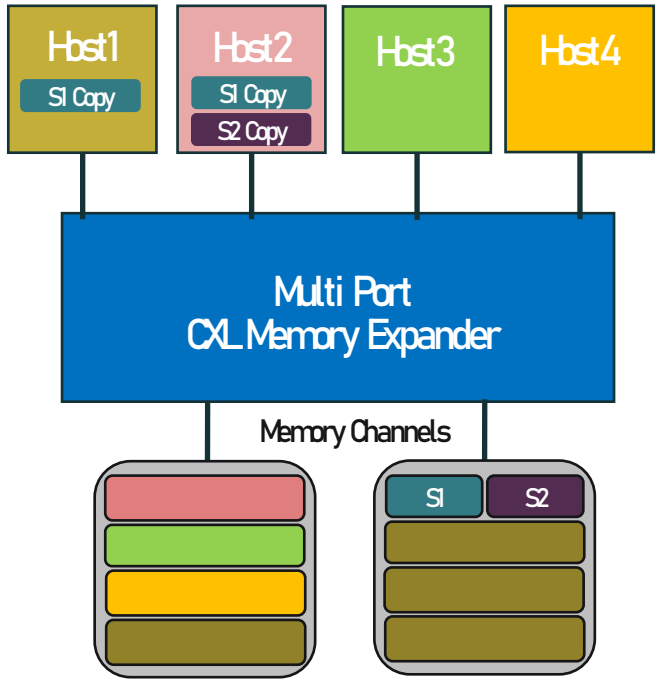
CXL Memory Expansion

- Improves processor efficiency
- Increases Capacity
- Improves Bandwidth
- Lowers TCO



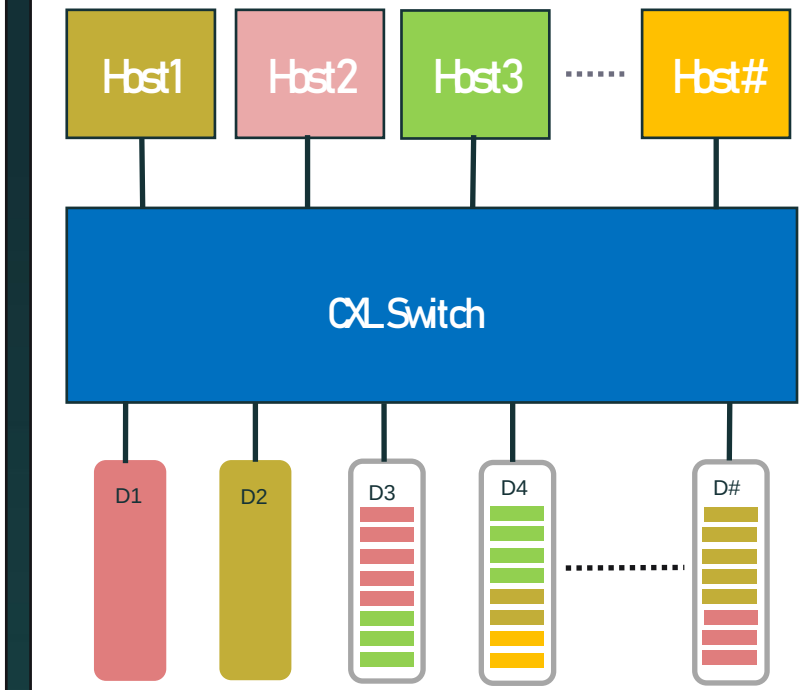
CXL-Enabled Tiered Expansion

- Flexible support for faster-slower Memory Tier
- Lowers TCO- higher memory capacity for cheaper $/GB
- Improves Bandwidth



Pooled Memory *Shared Memory*

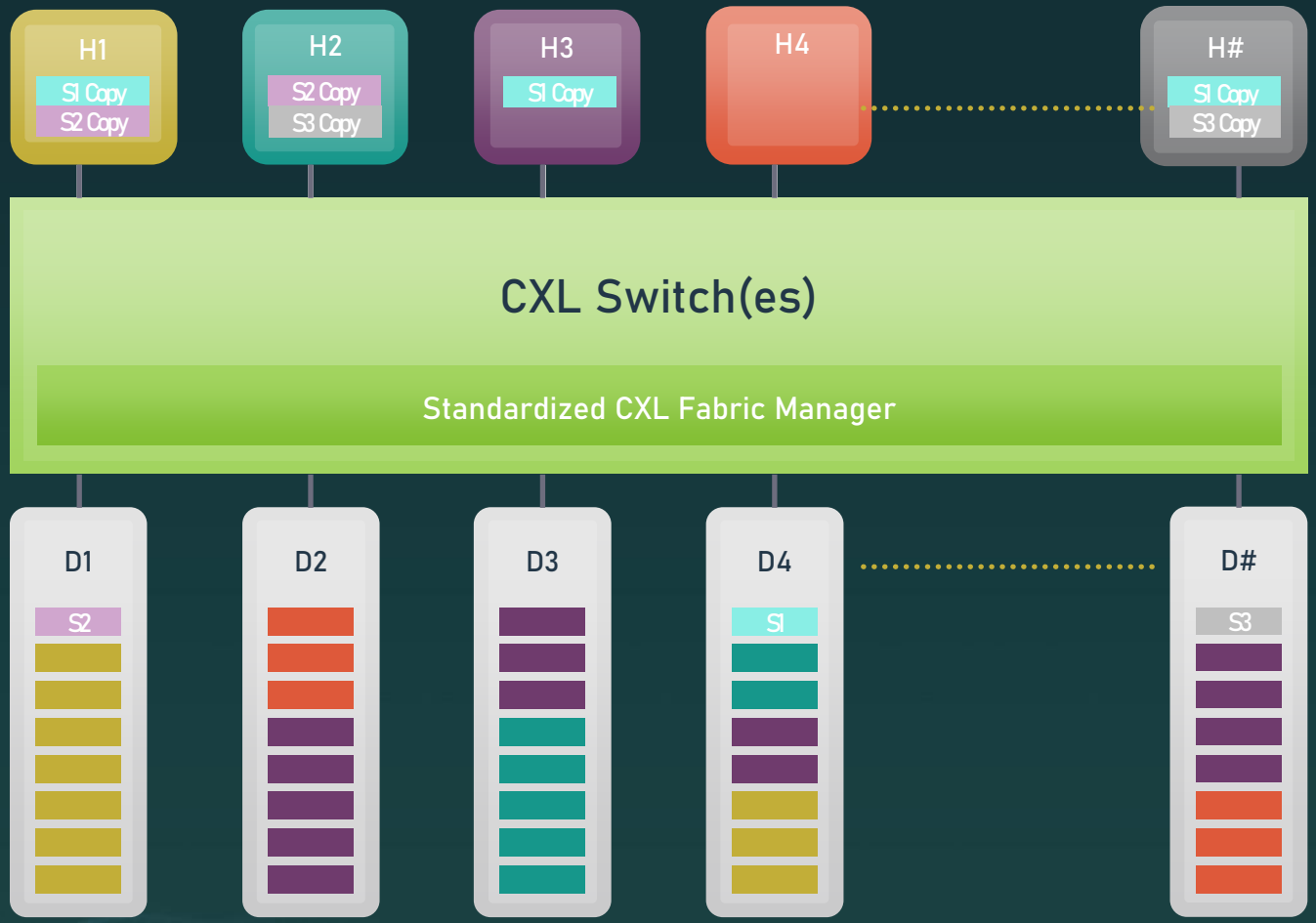
- Reduces Memory Stranding
- Improves Data Flow Efficiency
- Improves Memory Utilization
- Lowers TCO



CXL Switch with SLD and MLD

- Scales to large datasets
- Flexibility across the fabric
- Improves Memory Utilization
- Lowers TCO

Memory Pooling & Sharing



- Memory Pooling allows a host or multiple hosts to expand their memory capacity and bandwidth by using unique areas in a memory device with allocation of Memory segments tied to a unique host established at boot or a hot-swap event (i.e. memory segments accessed by a single host at runtime but can be migrated from host to host as needed).
- Memory Sharing allows multiple hosts to coherently share a common memory area in one or multiple memory devices. Multiple hosts can concurrently access and operate on that shared memory.

CXL Demos at SC'22

CXL Memory Solutions

AMD	AsteraLabs	Elastics.CLOUD	Microchip	Rambus	Samsung	Unifabrix
AMD SEV Enabled Confidential Containers on CXL Encrypted Memory	CXL from Promise to Reality with Real Silicon on Customer Platforms	Rack-Scale Memory Pooling with CXL	CXL-based SMC 2000 Smart Memory Controllers	CXL Memory Expansion with Intel Archer City PDK	AL/ML Application on CXL Memory Expander with Scalable Memory Development Kit (SMDK)	CXL-based Smart Memory Node™

CXL Demos at SC'22

CXL IP. Compliance and Testing

CXL™ Type 2 Compliance & Traffic Demo using 4th Gen Intel Xeon Scalable Processors and Intel FPGAs

Synopsys CXL 2.0 IP Successful Interoperability and Compliance Testing

CXL Fabric and Switch Solutions

Disaggregated and Composable CXL attached Memory Fabric

CXL Memory Pooling with a CXL Switch

CXL Software Solutions

Software for Memory Visualization, Tiering & Pooling

CXL at SC'22

- CXL is gaining momentum!
  - SC'21: 5 live CXL demos
  - SC'22: 12 live CXL demos
- CXL was recognized in the annual HPCWire Editors' Choice Award for Best HPC Interconnect Product or Technology
- View CXL technology demos: www.ComputeExpressLink.org/sc-22

Q&A Panel

CXL Demos at SC'22

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Thank You

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