PRESS RELEASE

CXL Consortium releases Compute Express Link 3.0 specification to expand fabric capabilities and management

Key highlights:

- The Compute Express Link™ (CXL™) 3.0 specification introduces fabric capabilities and management, improved memory sharing and pooling, enhanced coherency, and peer-to-peer communication.
- CXL 3.0 specification doubles the data rate to 64GTs with no added latency over CXL 2.0.
- The new specification is available to the public.
- CXL Consortium and its member companies will share key insights on CXL technology during Flash Memory Summit (FMS), August 2-4.

August 2, 2022 – Beaverton, OR – The CXL Consortium, an industry standards body dedicated to advancing Compute Express Link™ (CXL™) technology, today announced the release of the CXL 3.0 specification. The CXL 3.0 specification expands on previous technology generations to increase scalability and to optimize system level flows with advanced switching and fabric capabilities, efficient peer-to-peer communications, and fine-grained resource sharing across multiple compute domains.

"Modern datacenters require heterogenous and composable architectures to support compute intensive workloads for applications such as Artificial Intelligence and Machine Learning – and we continue to evolve CXL technology to meet industry requirements," said Siamak Tavallaei, president, CXL Consortium. "Developed by our dedicated technical workgroup members, the CXL 3.0 specification will enable new usage models in composable disaggregated infrastructure."

Highlights of the CXL 3.0 specification:

- Fabric capabilities
  - Multi-headed and Fabric Attached Devices
  - Enhanced Fabric Management
  - Composable disaggregated infrastructure
- Better scalability and improved resource utilization
  - Enhanced memory pooling
  - Multi-level switching
  - New enhanced coherency capabilities
  - Improved software capabilities
- Doubles the bandwidth to 64GTs
- Zero added latency over CXL 2.0
- Full backward compatibility with CXL 2.0, CXL 1.1, and CXL 1.0

"CXL 3.0 is a significant step forward in enabling heterogeneous computing," said Kevin Krewell, principal analyst, TIRIAS Research. "With its expanded features for coherent memory sharing and new fabric capabilities, CXL 3.0 adds new levels of flexibility and composability required by present day and future data centers. The CXL Consortium has made exceptionally fast progress in delivering this important spec to the industry."

CXL Consortium Presentations at Flash Memory Summit (FMS)
The CXL Consortium will introduce the new CXL 3.0 features at FMS, taking place August 2-4 at the Santa Clara Convention Center. View the FMS agenda for detailed information on the CXL presentations.

To schedule a meeting with a CXL representative during FMS, contact press@computeexpresslink.org.

Resources:

- CXL 3.0 specification
- CXL Consortium member statement of support
- CXL 3.0 white paper
- CXL 3.0 video

About the CXL™ Consortium
The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link™ (CXL™) technology. CXL is a high-speed interconnect offering coherency and memory semantics using high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

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