CXL™ Consortium Board of Directors – Statements of Support

Advanced Micro Devices Inc.
"AMD is excited about the expanded memory RAS and pooling capabilities in CXL 2.0. AMD is working as part of the CXL community to continuously improve this important technology which enables a tighter coupling and coherency between processors, accelerators and storage devices. We also look forward to CXL 3.0, which should add new capabilities and enable new use cases."
Nathan Kalyanasundharam, Senior Fellow, AMD

Alibaba
"Alibaba Cloud is delighted to support the launch of the CXL 2.0 specification. With the addition of CXL switching, CXL 2.0 has even better scale-up capabilities than previous revisions. As a technology innovator on cloud infrastructure and computing, Alibaba will explore how to leverage CXL technologies to benefit our customers and the community at large."
Di Xu, Chief Server Architect, Alibaba Infrastructure Service, Alibaba Cloud

Arm Limited
"Standardization is vital as the industry moves toward heterogenous compute solutions to power workloads such as machine learning, networking, storage and graphics. Arm is pleased to contribute to the CXL 2.0 specification to better support the performance demands of these workloads while also enabling enhanced interoperability and easing friction for CXL development across the vast Arm ecosystem."
Richard Grisenthwaite, Senior Vice President, Chief Architect, and Fellow, Arm

Cisco
"At Cisco, we believe the full potential of CXL 2.0 leads to simplification of computing and the operational model for IT teams. The consumption of compute resources will become much more dynamic and directly tied to workload needs driven by an AI powered orchestration vehicle. CXL 2.0 will help customers utilize infrastructure that has more direct optimization for the workloads that utilize them (i.e. accelerators, storage, memory) with a maximum in component utilization at scale. CXL 2.0's support for pooling memory devices will help in disaggregating and sharing efficiently in a cluster. These methods need to exist in an open framework for not only interoperability, but the orchestration and analytics to realize true benefit."
Dan Hanson, CTO, Cisco Cloud and Compute Technology Office

Dell
"With the development of the CXL 2.0 specification, the addition of switching and memory pooling are critical to the system environments needed for modern workloads as we continue to usher in memory-centric environments. Dell Technologies actively participates in and encourages the collaboration between CXL and Gen-Z that will allow customers to expand their composable architectures."
Praveen Vishakantaiah, Senior Vice President, CTO, Server & Infrastructure Systems, Dell EMC

Facebook
"The release of the CXL 2.0 specification highlights the strength, speed, and importance of open standards development. The switching, memory pooling, security, and common device interface improvements included in the CXL 2.0 release enable hyper-scale levels of memory-centric and

accelerator deployments. We look forward to continued innovation and collaboration on future CXL specifications for years to come."
Vijay Rao, Director of Technology and Strategy, Facebook

Google
"Google is excited to see CXL 2.0 come to fruition with the collaborative efforts of numerous industry partners. The CXL 2.0 specification release will help build a robust ecosystem of Memory and Accelerator product offerings and contribute to enabling new innovations in system architecture."
Prakash Chauhan, Systems Architect, Google LLC

HPE
"The ever increasing compute demand for advanced analytics, artificial intelligence, machine learning and exascale-class supercomputing continue to demand innovation around high-performance cache-coherent architectures. Unlocking memory-semantics from the processor is core to this direction, in an industry standard fashion. The CXL 2.0 specification is an evolutionary next step providing such enhancements as switching support for multi-domain pooled memory allowing disaggregation to optimize memory resources and reduce under-utilized stranded memory. As a Promoter and active contributor to the CXL Consortium, HPE is pleased to see the continued progress and release of the CXL 2.0 specification."
Mike Woodacre, HPE Fellow, CTO High Performance Computer & Mission Critical Solutions, HPE

Intel Corporation
"CXL's rapid adoption into so many innovators' roadmaps speaks volumes about the value this new interconnect standard will deliver to the ecosystem. Intel looks forward to enabling the new capabilities of CXL 2.0 such as switching, disaggregated resource pools, managed hot plug, and enhanced security in our future Intel Xeon platforms."
Carolyn Duran, Vice President of Memory and I/O Technologies, Intel Corporation

Microchip Technology Inc.
"Microchip is proud of its technical contributions to the CXL 2.0 standard leveraging our PCIe switch and fabric expertise. The combined expertise across the ecosystem and the momentum behind CXL will enable the adoption of breakthrough memory-centric solutions, and we are excited to continue driving further innovation with our customers."
Larrie Carr, Technical Fellow, Microchip Technology

Microsoft
"Microsoft is looking forward to the release of version 2.0 of the CXL specification which will enable the next generation of Cloud Computing. Microsoft strongly believes in industry collaboration to drive innovation. We look forward to combining the efforts of the Consortium with our own accelerated hardware achievements to advance rapidly-growing workloads – from Deep Learning to High Performance Computing to Confidential Computing – for the benefit of our customers and the advancement of the industry."
Leendert van Doorn, Distinguished Engineer, Microsoft

Xilinx, Inc.
"CXL continues its momentum with the successful completion of the 2.0 version of its specification. CXL 2.0 has important updates including switching and pooled memory device support as well as enhanced

security and reliability. This represents the continued efforts by the members to make CXL more capable in addressing the needs of the data center."
Gaurav Singh, Corporate Vice President, Xilinx, Inc.

CXL Consortium Contributors – Statements of Support

Ampere Computing
"Ampere designed the industry's first cloud-native processor, Ampere® Altra™, to deliver predictable high-performance, scalability and flexibility with high bandwidth coherent interconnect. As a contributing member of CXL and a proponent of open ecosystems, Ampere is excited to see the continued evolution of the high speed interconnect standard with CXL 2.0. When CXL solutions are available, it will enable our customers and ecosystem partners to implement new uses cases with an open standard-based coherent interconnect to our processor."
Scott Tetrick, Distinguished Architect, Ampere Computing

Astera Labs, Inc.
"Astera Labs is ready to unlock the new performance capabilities of CXL 2.0 in support of customers advancing data-centric applications, including Artificial Intelligence, Machine Learning and the Cloud. As the leading provider of purpose-built connectivity solutions, we look forward to enabling the next wave of data center innovation by joining hands with CXL consortium and our customers."
Sanjay Gajendra, Chief Business Officer, Astera Labs, Inc.

GigaIO Networks
"GigaIO Networks is delivering the first open standard Composable Disaggregated Infrastructure (CDI) platform with our innovative rack-scale, data-centric networking technology. We believe the disruptive advantage of CXL 2.0 along with its broad industry support will help usher a new era of CDI for critical data center resources such as memory, accelerators and storage. CXL 2.0 will be instrumental in maximizing performance while minimizing wasted resources. As an early Contributor member to the CXL Consortium, GigaIO Networks looks forward to defining, driving and adopting CXL and continuing to create the most efficient rack-scale systems for our customers."
Niraj Mathur, Vice President of Product, GigaIO Networks

Intelliprop
"The release of the CXL 2.0 specification will provide the critical baseline feature set necessary for companies to launch CXL 2.0 compliant product development in earnest. CXL 2.0 will provide the critical processor port necessary to enable a significant datacenter architectural revolution. This has been a huge effort from all of the CXL Consortium member teams to make this happen in a short period of time. Congratulations to all."
Hiren Patel, CEO, IntelliProp Inc.

Keysight Technologies
"With the rapid increase in computational workloads driven by applications in Artificial Intelligence, Machine Learning, communication systems, and High Performance Computing, the industry is challenged to keep pace with delivering the computational power needed within the required cost and power targets. CXL 2.0 technology will usher in a new generation of high performance computer architectures based on PCI Express® technology. Keysight's end-to-end solutions for Generation 5 and 6 digital busses including high performance UXR series oscilloscopes and M8040A series bit error ratio

testers are enabling the industry leaders to land PCIe 5.0 based technologies such as CXL 2.0 as well as providing them the development platform enabling PCIe 6.0 and other PAM4 based technologies at speeds up to 64GB."
Joachim Peerlings, Vice President and General Manager, Network and Data Center Solutions Group, Keysight Technologies

Micron Technology, Inc.
"CXL 2.0 offers an unprecedented opportunity to deliver breakthroughs in data center platform capability aligned with top workload demands. As a leader in DRAM, 3D XPoint, and NAND, Micron is collaborating closely with other industry players to deliver on the promise of this innovation together."
Steve Pawlowski, Corporate Vice President of Advanced Computing and Emerging Memory Solutions, Micron

Mobiveil, Inc.
"Mobiveil is excited to be part of the CXL Consortium along with the leaders and innovators of the tech industry. We believe that the open standard interface that CXL represents will enable the next big breakthrough in performance for high performance computation and acceleration at the data centers. As a leading provider of design IP and solutions we are committed to bring CXL design IP and validation platforms at the earliest to the market to accelerate CXL technology adoption and product development."
Ravi Thummarukudy, CEO, Mobiveil, Inc.

Montage Technology Co., Ltd.
"Montage is delighted and excited to join the CXL initiative to offer high performance, scalable interconnect technology to meet the demanding requirements of data centers, cloud computing and AI applications. We look forward to contributing to the open collaboration with all CXL members in order to enable a rich ecosystem that will greatly benefit future computing, storage and networking systems."
Stephen Tai, General Manager, Montage Technology

NVIDIA Corporation
"CXL 2.0 enhances switching and scalability for memory expansion while maintaining compatibility with CXL 1.1 and PCI Express 5.0. We are proud to be a part of the CXL team to continue development towards a truly open coherent interface that is highly performant and easy to scale."
Barry Wagner, Director, Technical Marketing, NVIDIA

PLDA, Inc.
"Over the past months, we have observed great traction for the CXL technology among our customers. As pioneers in High Speed Interconnect IP, our expertise has been challenged to propose optimal architectures and solutions. This is why we have committed our resources to developing best-in-class IP for the CXL 2.0 specification. The CXL 2.0 Specification introduces new features and enables additional usage models beyond CXL 1.1, including security enhancements, support for persistent memory, single-level switching, multi-domain memory pooling, etc. Today, we are ready to deliver comprehensive IP solutions for the Compute Express Link™ 2.0 specification with a focus on latency, size, features and performance."
Stephane Hauradou, CTO and Product Marketing, PLDA

Samsung Electronics Co., Ltd.

“As a leader in providing innovative memory solutions, Samsung is excited to be a driving force in defining new memory architectures. With support for features such as memory pooling and synchronous load reporting, the release of the CXL 2.0 specification is a major milestone in enabling breakthrough memory performance to address data-intensive applications. We look forward to collaborating with our ecosystem partners to deliver next generation memory solutions based on the CXL standard.”
Dr. Sangjoon Hwang, Senior Vice President of Memory Product Planning, Samsung Electronics

Seagate Technology LLC
"For over 40 years, Seagate Technology has been a global leader driving industry standards. We are pleased to support the open development of the CXL standard. CXL is integral to the future of composable architectures, defining an interface that supports desired low latency constructs for compute acceleration, memory, and persistent store. We look forward to continued innovation around this new interface and the capabilities it affords to support the ever-expanding datasphere."
John Morris, Senior Vice President and CTO, Seagate Technology

SK hynix
“CXL is creating a new opportunity and breakthrough in the industry satisfying the needs for improved memory system performance and power. Hence, it is very much expected to become an essential part of future computing systems. SK hynix very much welcomes the release of the CXL 2.0 specification in that regard. Also, CXL 2.0 is an exciting opportunity to introduce a new way for bandwidth-capacity and persistent memory expansions, beyond what is possible with the existing memory system architecture today. As a leading memory solution provider, SK hynix is looking very much forward to play a pivotal role in bringing such products into the market, and providing such solutions to our end-customers together with our industry partners.”
Uksong Kang, Corporate Vice President of DRAM Product Planning, SK hynix

Shenzhen Tencent Computer Systems Company Limited
“The launch of the CXL 2.0 specification is a great milestone as it enables broader industry collaboration on flexible resource sharing, application specific acceleration and many more innovations in the future. Tencent is glad to be part of this industry-wide effort. Tencent will continue working with partners in the CXL ecosystem and bring more breakthrough technologies to our customers, as at Tencent we believe in the mission of value for users and tech for good.”
Yan Zhao, Distinguished Engineer, VP of Tencent Cloud, Tencent

SiPearl
“We are delighted to be joining the CXL Consortium. While we are developing the high-performance, low-power microprocessor to equip future European exascale supercomputers, our membership will help ensure excellence for our future clients, including major contracting authorities for high performance computing. It will offer them a platform that is open to the major future standards for their industries.”
Philippe Notton, Founder and CEO, SiPearl

SMART Modular Technologies, Inc.
“SMART Modular fully supports the release of CXL 2.0 which enables the attachment of high-speed, low-latency, coherent memory, storage and accelerator module solutions. SMART remains committed to designing, manufacturing and supplying high-performance, highly-reliable industry standard solutions for the data center and cloud servers of tomorrow.”

Bob Frey, Senior Director Engineering, SMART Modular Technologies

Sony Semiconductor Solutions Corporation
"Sony Semiconductor Solutions is pleased to collaborate with the datacenter leaders of CXL Consortium in specifying and promoting this open interface standard. We clearly see the opportunity to deliver innovative, high performance CXL connected memory products, that accelerate the emerging AI and data driven composable infrastructure."
Terushi Shimizu, President and CEO of Sony Semiconductor Solutions Corporation

Synopsys, Inc.
"As an active member of the CXL Consortium, Synopsys plays an important role in helping to develop the CXL specification, enabling us to deliver the industry's first complete CXL IP solution. By implementing the new CXL 2.0 features in our widely adopted and available DesignWare CXL IP, designers can further benefit from the cache-coherent, low-latency data communication interface in their AI accelerator and high-performance computing SoCs."
John Koeter, Senior Vice President of Marketing and Strategy for IP, Synopsys

Teledyne LeCroy
"Teledyne LeCroy is a leading provider of PCI Express and CXL Protocol test equipment for development, validation and compliance testing of high performance and accelerator devices and systems. CXL 2.0 builds on the CXL 1.1 specification and will bring better memory coherency, higher performance and reduced software stack complexity to the Industry, enabling new applications and markets. Teledyne LeCroy is committed to fully supporting testing of CXL 2.0 hosts and devices with up to 16 lanes and 32 GT/s data rates with a complete development system including protocol analysis tools, Exercisers that provide Host and Device emulation – including error injection, and Compliance Testing as defined in the CXL 2.0 Base specification. These tools will be critical for engineers working on firmware, driver and system software validation of CXL 2.0 products."
Joe Mendolia, Vice President of Marketing, Protocol Solutions Group, Teledyne LeCroy

University of New Hampshire Interoperability Lab (UNH-IOL)
"UNH-IOL is happy to see the continued progress of CXL with the release of CXL 2.0. At UNH-IOL we've always held that open standards produce the best solutions and the highest levels of adoption and interoperability. It's clear that CXL has prioritized interoperability and compliance in the specification development process, and we're excited to continue our engagement with CXL Consortium."
David Woolf, Datacenter Industry Lead, University of New Hampshire Interoperability Lab (UNH-IOL)

Western Digital
"Western Digital is pleased to support the launch of the CXL 2.0 specification. This enhanced specification will contribute significantly to the wide adoption of this interface for both accelerators and memory. Such a broadly supported interface specification that promises to play a critical role in the evolution of memory subsystem comes about rarely, and Western Digital is happy to play a key contributor's role in its development."
Richard New, Vice President of Research, Western Digital

CXL Consortium Industry Liaisons – Statements of Support

DMTF
"As part of the alliance relationship between DMTF and the Compute Express Link (CXL) Consortium, the two organizations continue to collaborate for the betterment of the industry. The CXL 2.0 specification enables the beginnings of that effort. We look forward to ongoing and future collaborations in regard to DMTF's Redfish standard as well as standards developed by DMTF's Platform Management Components Intercommunication working group."
Jeff Hilland, President, DMTF

Gen-Z Consortium
"The Gen-Z Consortium congratulates the CXL Consortium on the release of its 2.0 specification. We look forward to the continued collaboration between our two organizations in developing memory-sematic interconnect specifications for next-generation computing."
Kurtis Bowman, President, Gen-Z Consortium