CXL Consortium announces Compute Express Link 3.1 specification release

Key highlights:

- The Compute Express Link™ (CXL™) 3.1 specification introduces CXL fabric improvements and extensions, Trusted-Execution-Environment Security Protocol (TSP), and memory expander improvements.
- The new specification is available to the public.
- CXL Consortium members are showcasing live CXL technology demonstrations at Supercomputing 2023 (SC'23).

November 14, 2023 – Beaverton, OR – The CXL Consortium, an industry standards body developing and promoting an open coherent interconnect, today announced the release of the Compute Express Link™ (CXL™) 3.1 specification with improved fabric manageability to take CXL beyond the rack and enable disaggregated systems. The CXL 3.1 Specification builds on previous iterations to optimize resource utilization, create trusted compute environments as needed, extend memory sharing and pooling to avoid stranded memory, and facilitate memory sharing between accelerators.

"The CXL 3.1 specification incorporates new features requested by the CXL community to create disaggregated systems and keep up with high-performance computational workloads," said Larrie Carr, CXL Consortium President. "With the support of our members, we continue to develop and promote CXL technology to enable an interoperable ecosystem of heterogeneous memory and computing solutions."

Highlights of the CXL 3.1 specification feature

- CXL Fabric improvements and extensions
  - Fabric Decode/Routing requirements
  - Fabric Manager API definition for PBR (Port Based Routing) Switch
  - Host-to-host communication with Global Integrated Memory (GIM) concept
  - Direct P2P CXL.mem support through PBR Switches
- Trusted-Execution-Environment Security Protocol (TSP)
- Memory Expander Improvements
  - Extended Meta Data with support for up to 32-bits per cache line of host specific state
  - Improved visibility into CXL memory device errors
  - Expanded visibility and control over CXL memory device RAS (Reliability, Availability, Serviceability)
- Full backward compatibility with CXL 2.0, CXL 1.1, and CXL 1.0

CXL Consortium members to demo live technology solutions at SC'23

The Consortium will host demos at the CXL pavilion (Booth #1301) at Supercomputing 2023, November 14-16 at the Colorado Convention Center in Denver. Additionally, CXL Consortium representatives will participate in the following sessions:

- Birds of a Feather: Increasing Memory Utilization and Reducing Total Memory Cost Using CXL
  - November 14 from 12:15 pm - 1:15pm
  - Room 405-407
- Exhibitor Forum: Compute Express Link (CXL): Advancing Coherent Connectivity
  - November 16 from 2:00 pm - 2:30 pm
  - Room 503-504

Resources:

- CXL 3.1 specification
- CXL 3.1 white paper
- CXL Consortium member statement of support
- CXL Consortium member demos at SC'23

About the CXL™ Consortium

The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link™ (CXL™) – an open coherent interconnect technology. A high-speed interconnect offering coherency and memory semantics, CXL uses high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

Press contact:
Elza Wong
Nereus for CXL Consortium
press@computeexpresslink.org