CXL Consortium Members – Statements of Support for CXL 3.1 Specification

Astera Labs
"As an active contributor to the CXL Consortium and a leader in CXL connectivity solutions for cloud and AI infrastructure, we are excited about the CXL 3.1 specification's new fabric, security, and memory expansion improvements. We look forward to enhancing our Leo Smart Memory Controllers with these new features to support additional CXL use cases and continue to meet the demands of memory-intensive workloads at cloud-scale."
Ahmad Danesh, Associate Vice President, Product Management, Astera Labs

Dell
"Dell Technologies has been a strong supporter of CXL technologies since the CXL Consortium was formed, and we believe the capabilities enabled by the CXL 3.1 Specification will further grow the CXL ecosystem. We are actively engaged at the CXL board of directors, technical task force, and work group levels to ensure CXL standards are beneficial to the industry and our customers. Dell also is leading efforts with other industry standards groups to ensure CXL memory module and management standards are available. We see great value to the industry as technology approaches consolidate and CXL is embraced as the industry standard for memory expansion and cache coherent accelerators."
Stuart Berke, Fellow & VP, Dell Technologies

Hewlett Packard Enterprise (HPE)
"We're excited for the release of the CXL 3.1 specification, which introduces routing and communication enhancements within switched fabric-attached memory and accelerator configurations, enabling future disaggregated system architectures. As enterprise, high performance computing, and artificial intelligence workflows evolve and grow to be more data-intensive, it will be important to evaluate the scalability of memory-centric computing solutions with fabric-attached resources on performance, use cases and effectiveness in securing and maintaining access to that data. Extensions included in the CXL 3.1 specification enable a standards-driven approach to incorporate these solution attributes as next-generation technologies are deployed. HPE values the opportunity to contribute to another noteworthy CXL Consortium milestone."
Andrew Wheeler, HPE Fellow, Vice President and Director, Hewlett Packard Labs

Lenovo
"Lenovo is an active member of the CXL Consortium and we are committed to developing this important standard while helping build the ecosystem around the new CXL interconnect. We are excited to be part of developing solutions that enable a new era of data center performance and efficiency, working with the consortium to identify specifications that foster the growth and adoption of innovative CXL products into future Lenovo systems."
Greg Huff, Chief Technology Officer, Lenovo Infrastructure Solutions Group

Liqid
"On behalf of Liqid and our customers, we're very excited about the much-awaited CXL 3.1 release. The introduction of the Fabric Manager marks a significant milestone, setting the stage for the disaggregation and composition of memory. This pivotal advancement will empower organizations to maximize their capacity footprints, unlocking extraordinary resource utilization and cost efficiencies. We firmly believe this is a giant leap forward in reshaping the future of computing infrastructure. We look forward to witnessing the transformative impact this will have on infrastructure worldwide."
Sumit Puri, CEO and Co-Founder, Liqid

Microchip
"As a contributing member of the CXL Consortium, Microchip recognizes the strategic value of an open industry standard like CXL. It can facilitate AI, ML and HPC applications by increasing the memory capacity available per core as well as increasing memory bandwidth per socket while improving memory resource utilization with pooling, sharing and scaled fabric attached memory use cases. Overall, the CXL 3.1 release provides increased functionality enabling the industry to support improved levels of efficiency and performance to the data center."
Samer Haija, Director of Marketing, Data Center Solutions Business Unit, Microchip

Micron
"Micron is proud to have contributed to the release of CXL 3.1, which adds security enhancements through the Trusted Execution Environment Security Protocol (TSP) to CXL memory and improves fabric-attached memory support introduced in this new standard. These exciting enhancements will allow the industry to solve the large data challenges of tomorrow and beyond, allowing vast amounts of memory to be addressed by a single host and shared by multiple hosts."
Vijay Nain, Senior Director of CXL Product Management, Micron

Google
"Google is pleased to support the release of the CXL 3.1 specification as it addresses critical Confidential Computing features required for cloud services. Furthermore, the specification enhances fabric related capabilities that could unlock new applications in the fast evolving machine learning infrastructure space."
Amit Nanda, Google and CXL Consortium Board Member

Rambus
"With the release of the CXL 3.1 specification, CXL continues to build momentum as a key technology in transforming memory in data centers. At Rambus, we are extremely proud to be members of the broad CXL ecosystem and committed to the development of solutions that will accelerate the adoption of CXL technology for new levels of data center performance and scalability."
Rami Sethi, General Manager of Memory Interface Chips, Rambus

Samtec
"Disaggregated computing, AI/ML, supercomputing, and other emerging usage models demand low-latency, high-speed and coherence. The CXL Consortium and member companies are collaborating on technical specifications helping overcome performance bottlenecks in existing memory system architectures. The new CXL 3.1 specification will drive memory architecture innovation and cache coherency adoption in chip-to-chip, PCB-to-PCB and rack-to-rack memory, storage, and accelerator applications."
Matthew Burns, Global Director of Technical Marketing, Samtec

SK hynix
"As a leading provider of most advanced and innovative memory and storage technologies, SK hynix is proud to be a part of CXL Consortium. As we contributed to the development of CXL3.1 specification especially on the memory features required for CXL memory modules, SK hynix absolutely congratulates the completion of CXL3.1 specification, which will be a key ingredient in building robust CXL memory devices with several use cases such as memory expansion, tiering, pooling, and switching. With various prototypes and engineering samples available, SK hynix is ready to show CXL memory products to the industry, enabling and expanding the CXL ecosystem with robust value propositions for better TCO. Furthermore, SK hynix will continue to be a major contributor to CXL Consortium with leading activities in technical working groups for next specification works."
Uksong Kang, Vice President of Next Generation Product Planning, SK hynix

Synopsys
As an active member of the CXL Consortium, Synopsys is helping to drive broad industry adoption of the CXL 3.1 specification with the industry's most trusted IP solutions. By providing a complete and compliant CXL IP offering including PHY, controller, verification IP and IDE security modules, Synopsys enables designers to efficiently develop high-performance SoCs with significantly less risk."
John Koeter, Senior Vice President of Marketing and Strategy for IP, Synopsys

VIAVI
"VIAVI congratulates the CXL Consortium on the release of its CXL 3.1 specification. This specification enables a new generation of advanced memory and AI applications that will revolutionize data center computing—and VIAVI is proud to support these initiatives."
Tom Fawcett, Senior Vice President and General Manager, Lab & Production, VIAVI

Western Digital
"Western Digital is pleased to support the release of CXL 3.1 specification. This version of specification provides significant enhancements to CXL 3.0 specifically in the areas of fabric attached memory and trusted computing. This represents another major milestone in the rapidly evolving CXL specification. With its introduction, the promise of memory disaggregation as well as sharing and pooling memory across servers can now be realized. This makes CXL a primary, rack-level system memory interface and presents an exciting opportunity to rethink datacenter architecture. Western Digital is proud to be an active, contributing member of this consortium."
Raj Ramanujan, distinguished engineer, Advanced Memory & CXL System Research, Western Digital

Xconn Technologies
"Xconn Technologies is thrilled about the release of CXL 3.1. As a pioneer in CXL switching, Xconn Technologies has been working with the CXL Consortium partner companies to fulfill a CXL 2.0 ecosystem with its revolutionary switch IC to enable CXL ecosystem and memory expansion, pooling and sharing applications. CXL 3.1 defines an architecture and feature set to boost AI computing, significantly expanding the landscape of applications. XConn Technologies has an industry leading product roadmap to support CXL 3.1 switching, we look forward to working with our partner companies on this exciting technology."
Gerry Fan, President and CEO, Xconn Technologies Holdings Inc.

ZeroPoint Technologies
“ZeroPoint Technologies is an active contributor to the CXL Consortium, helping to address the vital requirements and feedback from our end customers in the Composable memory solutions domain. The Consortium's inclusive membership empowers startups like ours to provide state-of-the-art memory compression IP, seamlessly operating within the CXL 3.1 Specification, and effectively meet the industry's evolving demands."
Nilesh Shah, VP Business Development, ZeroPoint Technologies