PRESS RELEASE

CXL Consortium Showcases First Public Demonstrations of Compute Express Link Technology at Supercomputing 2021

News Highlights:

- CXL Consortium members including Astera Labs, Intel, IntelliProp, Samsung, Synopsys, Teledyne LeCroy and more will exhibit interoperable CXL-based solutions in Booth 1607 onsite and in the CXL Consortium virtual booth
- CXL Consortium will participate in a Birds of a Feather session at SC21 with industry liaisons Gen-Z Consortium™ and SNIA as well as CXL Consortium member Facebook and Microsoft

November 15, 2021 – Beaverton, OR – The CXL™ Consortium, an industry standards body dedicated to advancing Compute Express Link™ (CXL™) technology, will showcase growing momentum for CXL technology at Supercomputing (SC21), taking place at America's Center in St. Louis, Missouri and virtually November 15-18. The CXL specification enables a high-speed, efficient interconnect between the CPU and platform enhancements and workload accelerators, such as GPUs, FPGAs and other purpose-built accelerator solutions. 12 companies will be demonstrating their CXL solutions during the show, including multi-vendor demos that highlight the growing CXL ecosystem.

"These CXL demonstrations are an important milestone for our organization," said Barry McAuliffe, president, CXL Consortium. "When the CXL Consortium was founded two years ago, we had a vision to deliver to the industry an open standard that would accelerate next-generation data center performance. That vision has now become reality as multiple member companies are delivering CXL solutions showcasing interoperability between vendors and enabling a new ecosystem for high-performance, heterogeneous computing."

"We're excited that our members have come together to showcase the first live technology demonstrations of CXL at SC21, including solutions featuring memory expansion, end-point support, memory disaggregation and more," said Glenn Ward and Kurt Lender, MWG Co-Chairs, CXL Consortium. "The technology demonstrations will feature the first CXL hardware and will highlight use cases in the industry that will benefit from CXL's high speed, low latency, cache coherent interconnect."

CXL Demos at SC'21:

- **Elastics.Cloud – Proof of Concept: Memory Disaggregation Local, Expanded, and Remote Memory:** The Elastics.cloud demo video introduces its memory disaggregation and pooling solution based on the emerging CXL standard. Its Smart Interconnect solution will further enable the sharing of memory in heterogeneous compute environments, while improving the performance required by the most demanding workloads. Optimized for better component utilization and enhanced performance, Elastics.cloud will enable functionality across a tiered data center model, while lowering total cost of ownership at scale.
- **Cadence IP for CXL Interop Demonstration:** In this video demo, Cadence will demonstrate its Endpoint Controller IP for CXL 2.0 interoperating with a CXL Host Server platform. This video will show a successful CXL linkup with a protocol analyzer, configuration space read and write, and memory read and write.
- **GigaIO – The Future of Composability with CXL:** Before CXL, the entire server could be disaggregated into pools of resources (CPU, storage, accelerators), except for memory. This video traces the journey and outlines the new capabilities CXL 1.0 and 2.0 will add to the

composable space, namely, coherent memory pooling and memory sharing as part of a disaggregated data center rack.

- **IntelliProp – CXL Fabric Adaptor Bridge Demo:** Demonstration of CXL Fabric Adaptor and Fabric Attached memory which is managed using a prototype Fabric Manager software. The demonstration showcases the ability to dynamically bind fabric attached resources to a CXL Host Node using in-band management over CXL and fabric protocols.
- **Meta – CXL Type 3 Memory Device Demo**
- **Montage Technology MXC + Retimer Video:** The demo shows a FPGA Base POC of a CXL Type3 memory expander controller (MXC) supporting CXL.mem and CXL.io protocols. It integrates a CXL controller, a DDR4/5 memory controller & a RISC-V micro-processor, and supports interfaces including SMBus for Host, I3C/I2C for media side and an SPI interface for external SPI flash. A PCIe® 5.0 retimer is used to secure the link budget to meet the challenging signal integrity requirements for long PCIe 5.0 channel comprising PCB, connector and cable. It uses advanced signal conditioning techniques to compensate for the channel attenuation and remove the impacts of various jitter sources.
- **Multi-Vendor Complete CXL System Demonstration between Astera Labs, Intel, and Synopsys:** This multi-vendor demonstration shows robust CXL™ interoperability between an Intel Sapphire Rapids CPU, Astera Labs' Solstice 3U Riser Card with two Aries CXL Smart Retimers, and the Synopsys DesignWare CXL Controller IP, showing successful transmission of CXL.io, CXL.cache, and CXL.mem transactions.
- **Rambus – Demonstration of a CXL Interconnect on a FPGA-based Design:** This video demonstrates CXL.mem read/write accesses to Host-managed Device Memory (HDM) between an Intel Host CPU and the Rambus CXL 2.0 Device Controller implemented in FPGA. The demonstration setup features Intel's Pre-Production Xeon processor as a host, connected to an FPGA board instantiating Rambus' CXL 2.0 Controller and CXL.mem test design.
- **Samsung – Functional Integration of SAP HANA In-Memory-Database on Samsung's CXL Memory Expander:** Samsung Memory Expander is a new type of memory device that supports CXL.mem protocol over PCIe slot. The end-to-end integration validates CXL ecosystem from OS, Linux kernel, CXL device driver, CXL.mem transactions and CXL link protocol. Samsung's Memory Solution Lab will apply this key technology to solve challenges of scaling of memory and compute for its customers.
- **Synopsys – Demonstration of DesignWare® CXL IP:** This demonstration, a complete CXL end-to-end connection, shows successful data transfer between Synopsys' DesignWare CXL Root Complex and Endpoint Controller IP solutions with full speed trace and analysis provided by a Teledyne LeCroy CXL Analyzer.
- **Teledyne LeCroy – CXL Live Traffic Demonstration:** This demo shows Synopsys DesignWare CXL Root Complex IP interoperating with Synopsys DesignWare CXL Endpoint IP, using a Teledyne LeCroy CXL Analyzer to capture the data and verify behavior.
- **Teledyne LeCroy – CXL Compliance Demonstration:** This is a demonstration of the Teledyne LeCroy Summit T516 Protocol Analyzer and Summit Z516 Protocol Exerciser running CXL 2.0 Compliance tests. This uses the Teledyne LeCroy LinkExpert software to automate the entire process.

CXL Presentation at SC'21

The CXL Consortium will also participate in a Birds of a Feather session "CXL™ Consortium, Gen-Z Consortium™, SNIA and End-Users – Is Disaggregation of Systems the Future?" on November 17 from 12:15-1:15 pm CST in Location 225-226 and online. The panel of experts will discuss how the

disaggregation of systems and persistent memory are critical to the industry and is being enabled by the organizations' technologies.

To schedule a meeting with a CXL representative during SC21, contact press@computeexpresslink.org.

About the CXL™ Consortium
The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link™ (CXL™) technology. CXL is a high-speed interconnect offering coherency and memory semantics using high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

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