



PRESS RELEASE

CXL™ Consortium Releases Compute Express Link™ 2.0 Specification

CXL 2.0 adds new features to meet the performance demands of next-generation datacenters while maintaining backwards compatibility with CXL 1.1 and 1.0

November 10, 2020 – The CXL™ Consortium, an industry standards body dedicated to advancing Compute Express Link™ (CXL) technology, today announced the release of the CXL 2.0 specification. CXL is an open industry-standard interconnect offering coherency and memory semantics using high-bandwidth, low-latency connectivity between host processor and devices such as accelerators, memory buffers, and smart I/O devices. The CXL 2.0 specification adds support for switching for fan-out to connect to more devices; memory pooling for increased memory utilization efficiency and providing memory capacity on demand; and support for persistent memory – all while preserving industry investments by supporting full backwards compatibility with CXL 1.1 and 1.0.

“Datacenter architectures continue to evolve rapidly to support the growing demands of emerging workloads for Artificial Intelligence and Machine Learning, with CXL technology keeping pace to meet the performance and latency demands,” said Barry McAuliffe, president, CXL Consortium. “Designed with breakthrough performance and easy adoption as guiding principles, the CXL 2.0 specification is a significant achievement from our dedicated technical work group members.”

Key Highlights of the CXL 2.0 Specification:

- Adds support for switching to enable device fan-out, memory scaling, expansion and the migration of resources.
- Includes memory pooling support to maximize memory utilization, limiting or eliminating the need to overprovision memory.
- Introduces standardized fabric manager specification for inventory and resource allocation to enable easier adoption and management of CXL-based switch and fabric solutions.
- Provides standardized management of the persistent memory interface and enables simultaneous operation alongside DDR, freeing up DDR for other uses.
- Introduces managed hot-plug support to take a CXL device online or offline from the system.
- Adds link-level Integrity and Data Encryption (CXL IDE) to provide confidentiality, integrity and replay protection for data transiting the CXL link.
- Supports a wide variety of industry interconnect form factors and standardized management interfaces to ease implementation.
- Includes Compliance and Interoperability specifications and in-system testing to enable a robust and interoperable multi-vendor ecosystem.

“The CXL Consortium has moved with breathtaking speed to deliver its second generation CXL 2.0 spec, even before products incorporating the first generation CXL 1.0 and 1.1 specs have reached the market,” observed Nathan Brookwood, Research Fellow at Insight 64. “The new 2.0 features, including switching,

memory pooling and persistent memory support pave the way for fully disaggregated systems in which pools of accelerators, DRAM and persistent memory storage can be dynamically connected to any one of 16 host servers to meet application demands. These features will enable system designers to invent entirely new types of systems that architects could only dream about just a few years ago.”

The CXL 2.0 specification is available for public download at www.computeexpresslink.org/download-the-specification.

Additional Resources:

- [White Paper: Introducing the CXL 2.0 Specification](#)
- [CXL Consortium Member Company Statements of Support](#)

About the CXL™ Consortium

The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link™ (CXL) technology. CXL is a high-speed interconnect offering coherency and memory semantics using high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

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