Compute Express Link™ (CXL™)

August 2022

Errata for the Compute Express Link Specification Revision 3.0

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Errata for the Compute Express Link Specification Revision 3.0

Aug 30, 2022

Contents

Revision History

Revision	Description	Date
1.0	First Release: G1-G2	August 30, 2022

G1 Section 3.3.7 and Section 4.3, BIRsp PBR message requires SPID field

The specification is missing the SPID in the PBR-format version of the BIRsp message, and this field is required to make FAM device memory isolation secure. For G-FAM, the GFD uses the SPID to associate the BIRsp with its outstanding BISnp. For an LD-FAM MLD connected via a PBR Edge Port, the Edge Port uses the SPID to determine the appropriate LD-ID to use in an HBR-format BIRsp message going to the MLD, which may pass through one or more HBR switches below the PBR switch. The security model will be covered in later specification updates.

3.3.7 M2S Back-Invalidate Response (BIRsp)

The Back-Invalidate Response (BIRsp) message class contains response messages from the Master to the Subordinate as a result of Back-Invalidate Snoops. This message class is not supported in 68B Flit mode.

Table 3-37 M2S BIRsp Fields

Field	Width (Bits)			Description
	68B Flit	256B Flit	PBR Flit	
Valid	N/A	1		The valid signal indicates that this is a valid response
Opcode		4		Response type with encodings in Table 3-38
BI-ID		12	0	BI-ID of the device that is the destination of the message. See Section 9.14 for details on how this field is assigned to devices. Not applicable in PBR messages where DPID infers this field.
BITag		12		Tracking ID from the device
LowAddr		2		The lower 2 bits of Cacheline address (Address[7:6]). This is needed to differentiate snoop responses when a Block Snoop is sent and receives snoop response for each cacheline. For block response (opcode names *Blk), this field is Reserved.
DPID		0	12	Destination Port ID
SPID		0	12	Source Port ID
RSVD		9		
Total		**40**	**52~~40~~**	

4.3 CXL.cachemem Link Layer 256B Flit Mode

<Below are various tables and slot formats that need to need to reflect the larger PBR message size>

Table 4-14. 256B G-Slot Formats

Format	SlotFmt Encoding	HBR				PBR	
		Messages	Downstream	Upstream	Length in Bits (Max 124)	Messages	Length in Bits (Max 124)
G0	0000b	H2D REQ + H2D RSP	X		112	H2D Req	92
G1	0001b	3 H2D RSP	X		120	2 H2D RSP	96
G2	0010b	D2H Req + 2 D2H RSP		X	124	D2H REQ	96
G3	0011b	4 D2H RSP		X	96	3 D2H RSP	108
G4	0100b	M2S REQ	X		100	M2S Req	120
G5	0101b	3 M2S BIRsp	X		120	23 M2S BIRsp	10420
G6	0110b	S2M BISnp + S2M NDR		X	124	S2M BISnp	96
G7	0111b	3 S2M NDR		X	120	2 S2M NDR	96
G8	1000b	RSVD				RSVD	
G9	1001b						
G10	1010b						
G11	1011b						
G12	1100b	4 H2D DH	X		112	3 H2D DH	108
G13	1101b	4 D2H DH		X	96	3 D2H DH	108
G14	1110b	M2S RwD	X		104	M2S RwD	124
G15	1111b	3 S2M DRS		X	120	2 S2M DRS	96

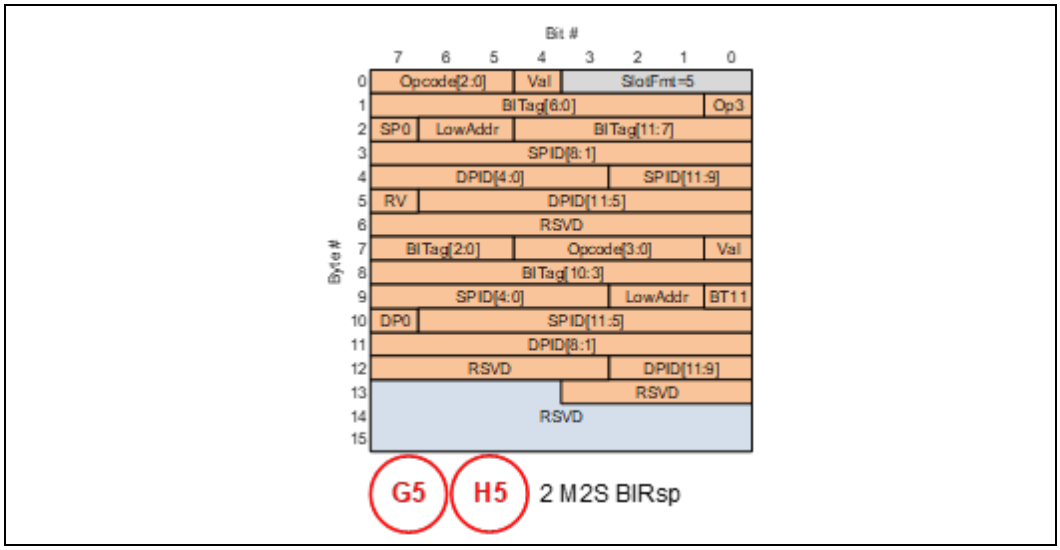
Table 4-15. 256B H-Slot Formats

Format	SlotFmt Encoding	HBR				PBR	
		Messages	Downstream	Upstream	Length in Bits (Max 108)	Messages	Length in Bits (Max 108)
H0	0000b	H2D REQ	X		72	H2D Req	92
H1	0001b	2 H2D RSP	X		80	2 H2D RSP	96
H2	0010b	D2H Req + 1 D2H RSP		X	100	D2H REQ	96
H3	0011b	4 D2H RSP		X	96	3 D2H RSP	108

H4	0100b	M2S REQ	X		100	M2S Req (Zero Extended)	108 (120)
H5	0101b	2 M2S BIRsp	X		80	2 M2S BIRsp	~~80~~104
H6	0110b	S2M BISnp		X	84	S2M BISnp	96
H7	0111b	2 S2M NDR		X	80	2 S2M NDR	96
H8	1000b	LLCTRL				LLCTRL	
H9	1001b	RSVD				RSVD	
H10	1010b						
H11	1011b						
H12	1100b	3 H2D DH	X		84	3 H2D DH	108
H13	1101b	4 D2H DH		X	96	3 D2H DH	108
H14	1110b	M2S RwD	X		104	M2S RwD (Zero Extended)	108 (124)
H15	1111b	2 S2M DRS		X	80	2 S2M DRS	96

<Figure below replaces the CXL3 figure>

Figure 4-57. 256B Packing: G5/H5 PBR Messages



G2 Latency-Optimized Empty Flits Allocate to Tx Retry Buffer

Currently, CXL.cachemem Empty flits are not allocated to the Tx Retry Buffer. This errata makes a change to allocate Latency-Optimized Empty Flits to the Tx Retry Buffer. Note, Standard Empty Flits are not impacted by this errata.

In Section 6.2.3.11, make the following update:

The 2 bytes of Flit Header as defined in Table 6-5 are transmitted as the first two bytes of the flit. The 2-bit Flit Type field indicates whether the flit carries CXL.io traffic, CXL.cachemem traffic, ALMPs, IDLE flits, Empty flits, or NOP flits. Please refer to Section 6.2.3.1.1.1 for more details. The Prior Flit Type definition is as defined in PCIe Base Specification; it enables the receiver to know that the prior flit was an non-retryable Empty flit, NOP flit, or IDLE flit, and thus does not require replay (i.e., can be discarded) if it has a CRC error. The Type of DLLP Payload definition is as defined in PCIe Base Specification for CXL.io flits; otherwise, this bit is reserved. The Replay Command[1:0] and Flit Sequence Number[9:0] definitions are as defined in PCIe Base Specification.

In Table 6-5, make the following update:

Table 6-5. 256B Flit Header

Flit Header Field	Flit Header Bit Location	Description
Flit Type[1:0]	[7:6]	• 00b = Physical Layer IDLE flit or Physical Layer NOP flit or CXL.io NOP flit • 01b = CXL.io Payload flit • 10b = CXL.cachemem Payload flit or CXL.cachemem generated Empty flit • 11b = ALMP Please refer to Table 6-6 for more details.
Prior Flit Type	[5]	• 0 = Prior flit was an non-retryable Empty, NOP, or IDLE flit (not allocated into Replay buffer) • 1 = Prior flit was a Payload flit or retryable Empty flit (allocated into Replay buffer)
Type of DLLP Payload	[4]	• If (Flit Type = (CXL.io Payload or CXL.io NOP): Use as defined in PCIe Base Specification • If (Flit Type != (CXL.io Payload or CXL.io NOP)): Reserved
Replay Command[1:0]	[3:2]	Same as defined in PCIe Base Specification.
Flit Sequence Number[9:0]	{[1:0], [15:8]}	10-bit Sequence Number as defined in PCIe Base Specification

In section 6.2.3.1.1.1, make the following update:

A Flit Type encoding of 10b indicates either a flit with valid CXL.cachemem Payload flit or a CXL.cachemem Empty flit; this enables CXL.cachemem to minimize idle to valid traffic transitions by arbitrating for use of the ARB/MUX transmit data path even while it does not have valid traffic to send so that it can potentially fill later slots in the flit with late arriving traffic, instead of requiring CXL.cachemem to wait until the next 256-byte flit boundary to begin transmitting valid traffic. CXL.cachemem Empty flits associated with standard 256B flits are non-retryable and must not be allocated into the transmit retry buffer or receive retry buffer. On the other hand, CXL.cachemem Empty flits associated with latency-optimized 256B flits are retryable and must be allocated into the transmit retry buffer.

Table 6-5. Flit Type[1:0]

Encoding	Flit Payload	Source	Description	Allocated to Retry Buffer?
00b	Physical Layer NOP	Physical Layer	Physical Layer generated (and sunk) flit with no valid payload; inserted in the data stream when its Tx retry buffer is full and it is backpressuring the upper layer or when no other flits from upper layers are available to transmit.	No
	IDLE		Physical Layer generated (and consumed) all 0s payload flit used to facilitate LTSSM transitions as described in PCIe Base Specification	No
	CXL.io NOP	CXL.io Link Layer	Valid CXL.io DLLP payload (no TLP payload); periodically inserted by the CXL.io link layer to satisfy the PCIe Base Specification requirement for a credit update interval if no other CXL.io flits are available to transmit.	No
01b	CXL.io Payload		Valid CXL.io TLP and valid DLLP payload	Yes
10b	CXL.cachemem Payload	CXL.cachemem Link Layer	Valid CXL.cachemem slot and/or CXL.cachemem credit payload	Yes
	CXL.cachemem Empty		No valid CXL.cachemem payload; generated when CXL.cachemem link layer speculatively arbitrates to transfer a flit to reduce idle to valid transition time but no valid CXL.cachemem payload arrives in time to use any slots in the flit.	If non-retryable: No If retryable: Allocate to Tx Retry Buffer only
11b	ALMP	ARB/MUX	ARB/MUX Link Management Packet	Yes