Compute Express Link™ (CXL™)

Engineering Change Notice to the Specification 2.0

July 2021

Add Mailbox Ready Time

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CXL ENGINEERING CHANGE NOTICE

TITLE:	Add mailbox ready time
DATE:	Introduced date (1/6/2021) Updated date (2/23/2021)
AFFECTED DOCUMENT:	CXL 2.0
SPONSOR:	Tiffany Kasanicky, Intel

Part I

1. **Summary of Functional Changes**

   This ECN extends the mailbox capabilities register to add a device advertised mailbox interface ready time.

2. **Benefits as a Result of the Changes**

   Provides a timeout value for device drivers to wait for the mailbox interface to be ready after a reset.

3. **Assessment of the Impact**

   CXL 2.0 specification did not specify a mailbox interface ready time. This change is backwards compatible.

Part II

Detailed Description of the Changes

8.2.8.4 Mailbox Registers (Offset varies)

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8.2.8.4.3 Mailbox Capabilities Register (Mailbox Registers Capability Offset + 00h)

Bits	Attributes	Description
4:0	RO	**Payload Size:** Size of the Command Payload Registers in bytes, expressed as 2^n. The minimum size is 256 bytes (n=8) and the maximum size is 1 MB (n=20).
5	RO	**MB Doorbell Interrupt Capable:** When set, indicates the device supports signaling an MSI/MSI-X interrupt when the doorbell is cleared. Only valid for the primary mailbox. This bit shall be zero for the secondary mailbox.
6	RO	**Background Command Complete Interrupt Capable:** When set, indicates the device supports signaling an MSI/MSI-X interrupt when a command completes in the background. Only valid for the primary mailbox. This bit shall be zero for the secondary mailbox.
10:7	RO	**Interrupt Message Number**: This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with this mailbox instance. Only valid for the primary mailbox. This bit shall be zero for the secondary mailbox. For MSI, the value in this field indicates the offset between the base Message Data and the interrupt message that is generated. Hardware is required to update this field so that it is correct if the number of MSI Messages assigned to the Function changes when software writes to the Multiple Message Enable field in the Message Control Register for MSI. For MSI-X, the value in this field indicates which MSI-X Table entry is used to generate the interrupt message. The entry shall be one of the first 16 entries even if the Function implements more than 16 entries. The value in this field shall be within the range configured by system software to the device. For a given MSI-X implementation, the entry shall remain constant. If both MSI and MSI-X are implemented, they are permitted to use different vectors, though software is permitted to enable only one mechanism at a time. If MSI-X is enabled, the value in this field shall indicate the vector for MSI-X. If MSI is enabled or neither is enabled, the value in this field indicate the vector for MSI. If software enables both MSI and MSI-X at the same time, the value in this field is undefined.
18:11	RO	**Mailbox Ready Time:** Indicates the maximum amount of time in seconds after a cold, warm, hot, or CXL reset for the Mailbox Interfaces Ready bit to become set in the Memory Device Status Register. A value of 0 indicates the device does not report a mailbox ready time.
31:~~11~~19	RsvdP	**Reserved**

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8.2.8.5 Memory Device Registers

8.2.8.5.1 Memory Device Status Registers (Offset Varies)

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8.2.8.5.1.1 Memory Device Status Register (Memory Device Status Registers Capability Offset + 00h)

Unless otherwise stated in the field definitions below, each field is present in version 1 and later of this structure. The device shall report the version of this structure in the Version field of the CXL Device Capability Header Register.

Bits	Attributes	Description
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4	RO	**Mailbox Interfaces Ready:** When set, the device is ready to accept commands through the mailbox register interfaces. Devices that report a non-zero mailbox ready time shall set this bit after a cold, warm, hot, or CXL reset within the time reported in the Mailbox Capabilities Register and it shall remain set until the next reset or the device encounters an error that prevents any mailbox communication.
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