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Compute Express Link™ (CXL™)

Engineering Change Notice to the Specification 2.0

July 2021

NULL CXL Capability ID

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CXL ENGINEERING CHANGE NOTICE

TITLE:	NULL CXL Capability ID
DATE:	Introduced date (03/09/2021) Updated date (03/30/2021)
AFFECTED DOCUMENT:	CXL 2.0
SPONSOR:	Mahesh Natu, Intel

Part I

1. Summary of Functional Changes

This ECN defines a NULL CXL Capability ID.

2. Benefits as a Result of the Changes

CXL 2.0 specification Table 142 defines a number of CXL Capability IDs that are used to identify group of registers in the CXL.cache and CXL.mem register block in CXL Component Register space. This ECN reserves the Capability ID=0 encoding as a NULL Capability ID, which the software will skip. This simplifies the hardware design if one or more CXL capabilities need to be made unavailable based on the configuration or the SKU. For example, CXL.cache and CXL.mem registers for CXL 2.0 device that supports CXL IDE may include the following Capability ID structures in this order

1 (Header), 2 (RAS), 4 (Link), 5 (HDM), 7 (IDE), Capability introduced by a future ECN

If this device is configured in CXL 1.1 mode, it is not permitted to expose IDE capability and must hide it. Without this ECN, the hardware may have to rearrange the structures and update the length field in the Header. With this ECN, the hardware designer could replace the Capability ID field in the IDE Capability structure with 0 to make the IDE capability disappear

1 (Header), 2 (RAS), 4 (Link), 5 (HDM), 0 (NULL), Capability introduced by a future ECN

3. Assessment of the Impact

This is an optional normative feature and as such, does not have any impact to existing hardware designs.

4. Analysis of the Hardware Implications

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This is an optional normative feature and as such, does not have any impact to existing hardware designs. It potentially simplifies hardware design in scenarios where one or more CXL capabilities need to be made unavailable based on the configuration or the SKU. Without this change, the hardware may have to rearrange CXL capability ID Structures if an structure in the middle of the array needs to be hidden.

5. Analysis of the Software Implications

Software is expected to skip CXL Capability ID structure it does not understand. Presently, CXL specification does not define ID=0, so this change is expected to be backwards compatible.

6. Analysis of the Compliance and Test Implications

CXL Capability List test should be updated to comprehend the Capability ID=0.

Part II

Detailed Description of the change

In Section 8.2.5 Table 142, make the following change

Capability	ID	Highest version	Mandatory[1]	Not Permitted	Optional
CXL NULL Capability – Software shall ignore this structure and skip to the next CXL Capability	0	Undefined		P	D1, D2, LD, FMLD, DP1, UP1, USP, DSP, R
..	..	..	..	..	..