Compute Express Link™ (CXL™)

Engineering Change Notice to the Specification 2.0

July 2021

Add vendor specific extension to Register Locator DVSEC

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CXL ENGINEERING CHANGE NOTICE

TITLE:	Add vendor specific extension to Register Locator DVSEC
DATE:	Introduced date (1/6/2021) Updated date (2/23/2021)
AFFECTED DOCUMENT:	CXL 2.0
SPONSOR:	Tiffany Kasanicky, Intel

Part I

1. **Summary of Functional Changes**

This ECN reserves a register block identifier in the Register Locator DVSEC for designated vendor specific register blocks and defines a fixed vendor specific register block header.

There may be errata in the Register Locator DVSEC that is not included in this ECN. Refer to the published errata for content that is not tracked as a change in this ECN.

2. **Benefits as a Result of the Changes**

This change allows device vendors to use the CXL specified mechanism to provide a pointer to vendor specific register blocks rather than defining a proprietary mechanism.

3. **Assessment of the Impact**

This is an optional feature. It will have no impact on existing implementations as the proposed vendor specific register block identifiers were marked as reserved in the CXL 2.0 spec.

The use of the PCI-SIG Vendor ID is not affected by the CXL agreement with the PCI-SIG regarding the CXL consortium's Vendor ID.

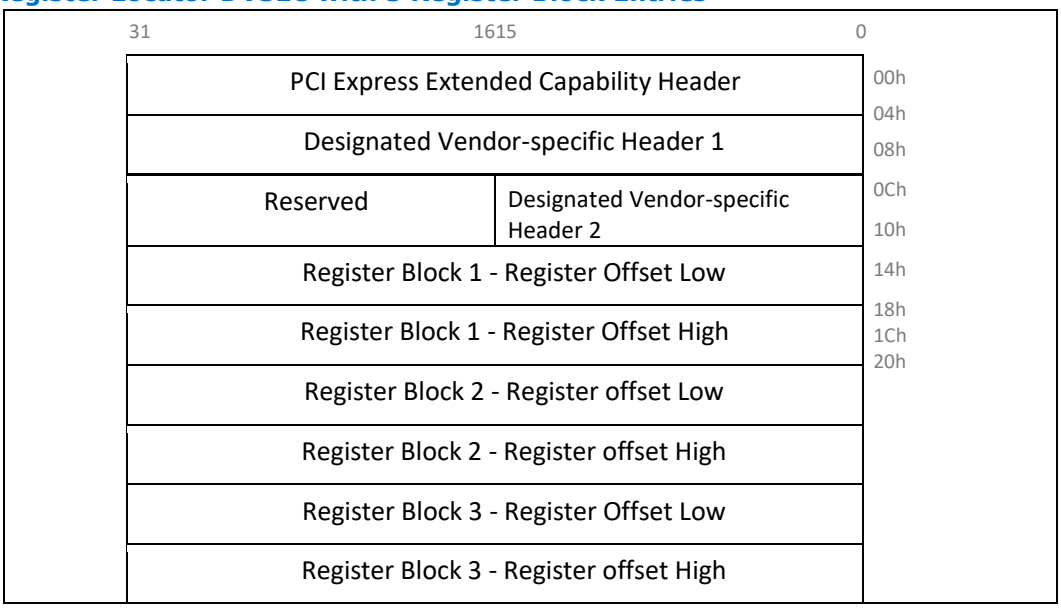
Part II

Detailed Description of the change

8.1.9 Register Locator DVSEC

The PCIe configuration space of a CXL 2.0 Root Port, CXL Downstream Switch Port, CXL Upstream Switch Port and CXL 2.0 Device must implement this DVSEC capability. This DVSEC capability contains one or more Register Block entries. Figure 131 illustrates a DVSEC Capability with 3 Register Block Entries. See Table 124 for the complete listing.

Figure 131. Register Locator DVSEC with 3 Register Block Entries



Each register block included in the Register Locator DVSEC has an Offset Low and an Offset High register to specify the location of the registers within the Memory Space. The Offset Low register includes an identifier which specifies the type of CXL registers. Each register block identifier shall only occur once in the Register Locator DVSEC structure, except for the Designated Vendor Specific register block identifier where multiple instances are allowed. Each register block must be wholly contained in the address range covered by the associated BAR.

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8.1.9.1 Register Offset Low (Offset Varies)

This register reports the BAR Indicator Register (BIR), Register Block Identifier and the lower address bits of the BAR offset associated with Register Block.

Bit	Attributes	Description
2:0	HwInit	Register BIR - Indicates which one of a Function's Base Address Registers, located beginning at 10h in Configuration Space, or entry in the Enhanced Allocation capability with a matching BAR Equivalent Indicator (BEI), is used to map the CXL Registers into Memory Space. Defined encodings are: • 0 Base Address Register 10h • 1 Base Address Register 14h • 2 Base Address Register 18h • 3 Base Address Register 1Ch • 4 Base Address Register 20h • 5 Base Address Register 24h All other Reserved. The Registers block must be wholly contained within the specified BAR.

7:3	RsvdP	Reserved.
15:8	HwInit	Register Block Identifier - Identifies the type of CXL registers. Defined encodings are: • 00h Indicates the register block entry is empty and the Register BIR, Register Block Offset Low and Register Block Offset High fields are invalid. • 01h Component Registers. The format of the Component Register block is defined in Section 8.2.4. • 02h BAR Virtualization ACL Registers. The format of the Component Register block is defined in Section 8.2.7. • 03h CXL Memory Device Registers. The format of the CXL Memory Device Register block is defined in Section 8.2.8. • FFh Designated Vendor Specific Registers. The format of the designated vendor specific register block starts with the header defined in Table X. All other Reserved.
31:16	HwInit	Register Block Offset Low - A[31:16] of offset from the address contained by one of the Function's Base Address Registers to point to the base of the Register Block. Register Block Offset is 64K aligned. Hence A[15:0] is zero.

Table X Designated Vendor Specific Register Block Header

Offset	Bit Location	Attributes	Description
00h	15:0	RO	Vendor ID - The PCI-SIG assigned Vendor ID for the organization that defined the layout and controls the specification for this register block.
00h	31:16	RO	Vendor Register Block ID - Value defined by the Vendor ID in bits 15:0 that indicates the nature and format of the vendor specific registers.
00h	35:32	RO	Vendor Register Block Revision - Version number defined by the Vendor ID in bits 15:0 that indicates the version of the register block.
00h	63:36	RsvdP	Reserved
08h	31:0	RO	Vendor Register Block Length - The number of bytes in the register block, including the Designated Vendor Specific Register Block Header and the vendor specific registers.
08h	63:32	RsvdP	Reserved