CXL Consortium™ Webinar

An Introduction to Compute Express Link™ (CXL) Technology
Agenda

• Presenter Introductions
• Introduction to Compute Express Link™
  • Industry Landscape
  • CXL Overview
  • CXL Features & Benefits
  • CXL Use Cases
• Introducing CXL Consortium™
  • CXL Consortium™ Origin & Incorporation
  • Membership Information
• Q&A
Today’s Presenters

Kurtis Bowman
CXL Consortium Board Member – Secretary
Director of Server Architecture and Technologies - Server Office of CTO at Dell EMC

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Fellow and Director of I/O Technology and Standards at Intel
Industry Landscape

Industry mega-trends are driving demand for faster data processing and next-generation data center performance

- **Proliferation of Cloud Computing**
- **Growth of AI & Analytics**
- **Cloudification of the Network & Edge**
Why the need for a new class of interconnect?

Extend PCIe® for heterogenous computing and disaggregation usages:

- Need a new class of interconnect for heterogenous computing and disaggregation usages:
  - Efficient resource sharing
  - Shared memory pools with efficient access mechanisms
  - Enhanced movement of operands and results between accelerators and target devices
  - Significant latency reduction to enable disaggregated memory
- The industry needs open standards that can comprehensively address next-gen interconnect challenges

Today’s Environment

CXL Enabled Environment

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Overview of Compute Express Link™
CXL Overview

• New breakthrough high-speed CPU-to-Device interconnect
  • Enables a high-speed, efficient interconnect between the CPU and platform enhancements and workload accelerators
  • Builds upon PCI Express® infrastructure, leveraging the PCIe® 5.0 physical and electrical interface
  • Maintains memory coherency between the CPU memory space and memory on attached devices
    • Allows resource sharing for higher performance
    • Reduced complexity and lower overall system cost
    • Permits users to focus on target workloads as opposed to redundant memory management

• Delivered as an open industry standard
  • CXL Specification 1.1 is available now
  • Future CXL Specification generations will continue to innovate to meet industry needs

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Introducing CXL

• Processor Interconnect:
  • Open industry standard
  • High-bandwidth, low-latency
  • Coherent interface
  • Leverages PCI Express®
  • Targets high-performance computational workloads
    • Artificial Intelligence
    • Machine Learning
    • HPC
    • Comms

A new class of interconnect for device connectivity
What is CXL?

• Alternate protocol that runs across the standard PCIe physical layer

• Uses a flexible processor port that can auto-negotiate to either the standard PCIe transaction protocol or the alternate CXL transaction protocols

• First generation CXL aligns to 32 Gbps PCIe 5.0

• CXL usages expected to be key driver for an aggressive timeline to PCIe 6.0
CXL Protocols

The CXL transaction layer is comprised of three dynamically multiplexed sub-protocols on a single link:

**CXL.io**
Discovery, configuration, register access, interrupts, etc.

**CXL.cache**
Device access to processor memory

**CXL.Memory**
Processor access to device attached memory
CXL Features and Benefits
CXL Stack – Designed for Low Latency

- All 3 representative usages have latency critical elements:
  - CXL.cache
  - CXL.memory
  - CXL.io

- CXL cache and memory stack is optimized for latency:
  - Separate transaction and link layer from IO
  - Fixed message framing

- CXL io flows pass through a stack that is largely identical a standard PCIe stack:
  - Dynamic framing
  - Transaction Layer Packet (TLP)/Data Link Layer Packet (DLLP) encapsulated in CXL flits

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CXL Stack – Design for Low Latency

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Asymmetric Complexity

CCI* Model – Symmetric CCI Protocol

CXL Model – Asymmetric Protocol

CXL Key Advantages:
• Avoid protocol interoperability hurdles/roadblocks
• Enable devices across multiple segments (e.g. client / server)
• Enable Memory buffer with no coherency burden
• Simpler, processor independent device development

*Cache Coherent Interface
Critical access class for accelerators is “device engine to device memory”

“Coherence Bias” allows a device engine to access its memory coherently without visiting the processor

Two driver managed modes or “Biases”

HOST BIAS: pages being used by the host or shared between host and device

DEVICE BIAS: pages being used exclusively by the device

Both biases guaranteed correct/coherent

Guarantee applies even when software bugs or speculative accesses unexpectedly access device memory in the “Device Bias” state.
CXL Use Cases
Representative CXL Usages

### Caching Devices / Accelerators

**Usages:**
- PGAS NIC
- NIC atomics

**Protocols:**
- CXL.io
- CXL.cache

### Accelerators with Memory

**Usages:**
- GPU
- Dense Computation

**Protocols:**
- CXL.io
- CXL.cache
- CXL.memory

### Memory Buffers

**Usages:**
- Memory BW expansion
- Memory capacity expansion
- Storage Class Memory

**Protocols:**
- CXL.io
- CXL.mem

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Heterogeneous Computing Revisited – with CXL

CXL enables a more fluid and flexible memory model
Single, common, memory address space across processors and devices

- More efficient population and update of operands
- More efficient extraction of results
- Memory resource “borrowing”
- User/Kernel level data access and data movement
- Low latency to memory, host to device and device to host

CPU-attached Memory
(OS Managed)

Accelerator-Attached Memory
(Runtime managed cache)

PCIe DMA

Writeback Memory

Memory Load/Store

CPU attached Memory
(Os Managed)

CPU

Writeback Memory

Memory Load/Store

CPU

CPU

GPU

FPGA

AI

NIC

NIC

PCIe DMA

Writeback Memory

Memory Load/Store

PCIe DMA

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CXL Summary

CXL has the right features and architecture to enable a broad, open ecosystem for heterogeneous computing and server disaggregation:

**Coherent Interface:**
Leverages PCIe® with 3 mix-and-match protocols

**Low Latency:**
.Cache and .Mem targeted at near CPU cache coherent latency

**Asymmetric Complexity:**
Eases burdens of cache coherent interface designs

**Open Industry Standard:**
With growing broad industry support
Introducing CXL Consortium™
Introducing CXL Consortium™

- Alibaba, Cisco, Dell EMC, Facebook, Google, Hewlett Packard Enterprise, Huawei, Intel Corporation and Microsoft announced their intent to incorporate in March 2019.

- This core group announced incorporation of the Compute Express Link (CXL) Consortium on September 17, 2019 and unveiled the names of its Board of Directors:
Membership Overview

• CXL Consortium™ boasts 90+ member companies to date and is growing rapidly
  • Current membership ranks reflects the required industry expertise to create a robust, vibrant CXL ecosystem

• Two levels of membership are available for participation in CXL
  • Adopter memberships are free and allow your company to:
    • Access the final specification releases
    • Gain IP protection as outlined in the IPR Policy and Membership Agreements
  • Contributor membership are $20K for the first year and $10K per year each subsequent year with the following added benefits:
    • Participate in the CXL workgroups
    • Influence the direction of the technology
    • Access the intermediate specifications (dot level releases)
Membership Overview

• Members have access to the CXL Specification 1.1
  • Both the Host and Target side of the interface is published
  • All members can implement the spec under the Consortium’s IP protection policy
• An evaluation copy of the 1.1 Spec is available at computeexpresslink.org
• The CXL Consortium will deliver future generations of the Specification
  • Contributor members can participate in the definition and promotion of future specifications in the CXL Working Groups:
    • Compliance WG
    • Marketing WG
    • Memory System WG
    • PHY WG
    • Protocol WG
    • Software & Systems WG
• CXL maintains backwards compatibility to protect member investments
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Q&A