CXL ENGINEERING CHANGE NOTICE

TITLE:	Addition for performance monitoring events for CXL memory devices
DATE:	Introduced date: 3/20/2024
AFFECTED DOCUMENT:	CXL 3.1
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Part I

1. **Summary of Functional Changes**
   This ECN defines additional set of performance events to be included as part of CXL performance monitoring unit (CPMU) definition.

2. **Benefits as a Result of the Changes**
   Enhanced performance telemetry to be available at system level for CXL device performance, especially for CXL memory devices which are part of system memory.
3. **Assessment of the Impact**
   This is an optional feature. It will have no impact on existing implementations.

4. **Analysis of the Hardware Implications**
   This is an optional normative feature. The CXL components supporting CPMU may add additional event counters and advertise in CPMU capabilities.

5. **Analysis of the Software Implications**
   This is an optional normative feature. To take advantage of this feature, software will be required to discover and configure the bits as described in this document.

6. **Analysis of the Compliance and Test Implications**
   This ECN does not repurpose any reserved bits and as such, does not impact existing C&I tests.

Part II

Detailed Description of the change

Section 13.2

Addition to Table 13-5

Event Group	Event Id	Mnemonic	Event Description	Filters	MEC
8000h (DDR Interface)2	00h	ACT Count	Counts the number of DRAM Activate commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	Add
	01h	PRE Count	Counts the number of all DRAM Precharge commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	02h	CAS Rd	Counts the number of all DRAM Column Address Strobe read Commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	

	03h	CAS Wr	Counts the number of all DRAM Column Address Strobe write commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	04h	Refresh	Counts the number of all DRAM Refresh commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	05h	Self Refresh Entry	Counts the number of Self Refresh Entry commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	06h	RFM	Counts the number of Refresh Management (RFM) commands that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	07h	CAS Rd AP	Counts the number of DRAM Column Address Strobe read Commands with Auto Precharge that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	08h	CAS Wr AP	Counts the number of DRAM Column Address Strobe write Commands with Auto Precharge that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	09h	Refresh All Banks	Counts the number of DRAM Refresh All banks that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	0Ah	Refresh Same Bank	Counts the number of DRAM Refresh Same banks that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	0Bh	Power Down Entry	Counts the number of DRAM Power down Entry that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	0Ch	Power Down Exit	Counts the number of DRAM Power down Exit that were issued by the Memory Controller associated with this CPMU.	Filter ID=1	
	Dh	RD/WR DDR bus switching	count the number of times -Read to write or vice versa DDR bus mode switching (DDR turnarounds) for memory controller bus	Filter ID=1	
	0Eh	Incoming Read requests	Command count for incoming read requests at memory controller interface. The event is supported only in CPMU associated with memory controller block. Memory controller interface point and requests being counted are vendor specific, additional vendor-supplied information may be needed.	Filter ID=1	
	0Fh	Incoming write requests	Command count for incoming write requests at memory controller interface. The event is supported only in CPMU associated with memory controller block. Memory controller interface point and requests being counted are vendor specific, additional vendor-supplied information may be needed.	Filter ID=1	
	10h-1Fh	Reserved	Reserved		
8001h (Queue occupancy)	0h	RD Queue Occupancy	# of clock cycles read queue occupied is above the specified threshold in the counter configuration. The event is supported only when the controller implements separate read and write queues.	Filter ID=1	NA
	1h	WR Queue Occupancy	# of clock cycles write queue occupied is above the specified threshold in the counter configuration. The event is supported only when the controller implements separate read and write queues.	Filter ID=1	NA
	2h	Rd/WR merged Queue Occupancy	# of clock cycles merged RD/WR queue occupied is above the specified threshold in the counter configuration. The event is supported only when the controller does not implement separate read and write queues.	Filter ID=1	NA
	03h	pwrdn event	CKE power down cycles or residency in PDN state (# of clocks)	Filter ID=1	NA

	4-1Fh	Reserved	Reserved		
8002h(Queue Residency)	0h	Memory controller Read residency count	The accumulative number of clock cycles there is any outstanding read pending for completion to be sent out from memory controller. This counter can be used to determine average latency over large number of transactions when combined with command counts	Filter ID=1	NA
	1h	Memory controller write residency count	The accumulative number of clock cycles there is any outstanding write pending for completion to be sent out from memory controller. This counter can be used to determine average latency over large number of transactions when combined with command counts	Filter ID=1	NA
	02h-1Fh	Reserved	Reserved		
8003h(Retry Events)	0h	Retry event triggered by read crc	Count the retry event triggered by listed error event for the memory controller associated with this CPMU. Include host issued transaction and/or internal (patrol scrub)	Filter ID=1	ADD
	1h	Retry event triggered by write crc	Count the retry event triggered by listed error event for the memory controller associated with this CPMU. Include host issued transaction and/or internal (patrol scrub)	Filter ID=1	ADD
	2h	Retry event triggered by CA parity	Count the retry event triggered by listed error event for the memory controller associated with this CPMU. Include host issued transaction and/or internal (patrol scrub)	Filter ID=1	ADD
	3h	Retry event triggered by ECC	Count the retry event triggered by listed error event for the memory controller associated with this CPMU. Include host issued transaction and/or internal (patrol scrub)	Filter ID=1	ADD
	4h-1Fh	Reserved	Reserved		
8004h (Throttle Events)	0h	Thermal Throttle event	Count of cycles (# of clocks) when the CXL memory device is in any thermally throttled state (throttle state definition is left to implementation choice)		NA
	1h	Power Throttle event	Count of cycles (# of clocks) when the CXL memory device is in any power throttled state (throttle state definition is left to implementation choice)		NA
	2h-1fh	Reserved	Reserved	NA	NA
8005h-FFFFh	Reserved	Reserved	Reserved	NA	NA
26h-2Fh	Reserved	Reserved	Reserved	NA	NA
30h(Devload)	Devload encoding	Devload signaled by the device	Count the # of clock cycles the device is in devload= event ID condition		NA
31h(M2S Residency)	0h	M2S Req residency count	The accumulative number of clock cycles there is any outstanding M2S Req pending for completion to be sent out to host. This counter can be used to determine average latency over large number of transaction when combined with command counts		NA

	1h	M2S RwD residency count	The accumulative number of clock cycles there is any outstanding M2S RwD pending for completion to be sent out to host. This counter can be used to determine average latency over large number of transaction when combined with command counts		NA
	2h-1Fh	Reserved	Reserved		
32h-7FFFh	Reserved	Reserved	Reserved	NA	NA