CXL Consortium Announces Compute Express Link 3.2 Specification Release

Key highlights:

- Compute Express Link® (CXL®) 3.2 Specification enhances security, compliance, and functionality of CXL Memory Devices.
- New, fully backward compatible specification is now available to the public.

December 3, 2024 – Beaverton, Ore. – The CXL Consortium, an industry standard body advancing coherent connectivity, announces the release of its Compute Express Link® (CXL®) 3.2 Specification. The 3.2 Specification optimizes CXL Memory Device monitoring and management, enhances functionality of CXL Memory Devices for OS and Applications, and extends security with the Trusted Security Protocol (TSP).

"We are excited to announce the release of the CXL 3.2 Specification to advance the CXL ecosystem by providing enhancements to security, compliance, and functionality of CXL Memory Devices," said Larrie Carr, CXL Consortium President. "The Consortium continues to develop an open, coherent interconnect and enable an interoperable ecosystem for heterogeneous memory and computing solutions."

Highlights of the CXL 3.2 Specification:

- Optimized CXL Memory Device monitoring and management
  - New CXL Hot-Page Monitoring Unit (CHMU) for memory tiering
  - Common event record
  - Compatibility with PCIe Management Message Pass Through (MMPT)
  - CXL online firmware (FW) activation capabilities
- Enhanced functionality of CXL Memory Devices for OS and Application
  - Post Package Repair (PPR) enhancements
  - Additional performance monitoring events for CXL Memory Devices
- Extends security with the Trusted Security Protocol (TSP)
  - New Meta-bits Storage Feature for Host-only Coherent Host-Managed Device Memory (HDM-H) address regions
  - Improved security by expanding IDE protection
  - Increases security of Host-only Coherent Device-Managed Memory with Back-Invalidation (HDM-DB) memory devices
  - Enhances compliance tests for interoperability
- Full backward compatibility with all previous CXL specifications

Resources:

- CXL 3.2 Specification
- Opportunities and Challenges of Compute Express Link (CXL) White Paper by ABI Research

About the CXL Consortium

The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link® (CXL®) – an open coherent interconnect technology. A high-speed interconnect offering coherency and memory semantics, CXL uses high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

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