CXL Consortium Releases the Compute Express Link 4.0 Specification Increasing Speed and Bandwidth

Key highlights:

- CXL 4.0 specification doubles bandwidth from 64GTs to 128GTs, adds support for bundled ports, and enhances memory RAS features.
- The new specification is released to the public.
- CXL Consortium members are showcasing live CXL technology demonstrations at Supercomputing 2025 (SC25).

BEAVERTON, Ore., Nov. 18, 2025 – CXL Consortium, the industry standard organization developing and promoting an open coherent interconnection for heterogeneous memory and computing solutions, today announced the release of the Compute Express Link® (CXL®) 4.0 specification to meet the increasing demands of emerging workloads placed on today's data centers.

"The release of the CXL 4.0 specification sets a new milestone for advancing coherent memory connectivity, doubling the bandwidth over the previous generation with powerful new features," said Derek Rohde, CXL Consortium President and Treasurer, and Principal Engineer at NVIDIA. "This release reflects our member companies' commitment to driving open standards that empower data center innovation, support compliance and interoperability, and enable the entire industry to scale for future usage models."

Key features of the CXL 4.0 specification

- Doubles the bandwidth to 128GTs with zero added latency
  - Enables rapid data movement between CXL devices, directly improving system performance
  - Maintains previously enabled CXL 3.x protocol enhancements with the 256B Flit format
  - Introduces the concept of native x2 width to support increased fan-out in the platform
  - Support for up to four retimers for increased channel reach
- Implements CXL bundled port capabilities
  - Ability to combine device ports between Host and CXL accelerators (Type 1/2 devices) to increase bandwidth of the connection
- Delivers memory RAS enhancements
  - Improves reliability, error visibility, and maintenance efficiency
- Continued full backward compatibility with CXL 3.x, 2.0, 1.1, and 1.0

Meet CXL Consortium representatives and members at SC'25
The CXL Consortium will host demos at the CXL Pavilion (Booth #817) at Supercomputing 2025 (SC'25), November 16-21, at the America's Center in St. Louis, MO. Additionally, CXL Consortium representatives are participating in the following session:

- Birds of a Feather: How to Leverage CXL Memory Pooling and Sharing for AI & HPC workloads on Tuesday, November 18, 12:15 – 1:15 pm PT

Take a deep dive into the CXL 4.0 Specification
The CXL Consortium Leadership and Technical Task Force are hosting a free live webinar on Thursday, December 4, at 8 am PT to introduce the new features of the CXL specification. Register for the webinar via Zoom Webinar.

Resources:

- CXL 4.0 specification
- CXL 4.0 white paper
- CXL Consortium Members – Statements of Support for the CXL 4.0 Specification

About the CXL Consortium
The CXL Consortium is an industry standards body dedicated to advancing Compute Express Link® (CXL®) – an open coherent interconnect technology. A high-speed interconnect offering coherent memory semantics, CXL uses high-bandwidth, low-latency connectivity between the host processor and devices such as accelerators, memory buffers, and smart I/O devices. For more information or to join, visit www.computeexpresslink.org.

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